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Notice to Authors: Address all papers and editorial correspondence to R. E. Meagher, 168 Engineering Research Laboratory, University of Illinois, Urbana, Ill. To avoid delay, 3 copies of papers and figures should be submitted, together with the originals of the figures which will be returned on request. All material will be returned if a paper is not accepted.

The Editor

Readers of the *PGEC Transactions* who regularly scan the not-so-fine print of the inside cover may have noticed the name of R. E. Meagher newly listed as the Editor in the June issue. Since the appointment was not settled until June 22nd, this was the fastest news coverage so far in the short history of the *Transactions*. The purpose of the last-minute change in the cover was to inform potential authors of the new editorial address. Unfortunately, we could not also make a more formal announcement in that short a time.

The function of the Editor is to act as the executive agent of the Editorial Board. He corresponds with the authors, sends papers out for review, and makes arrangements with the IRE Headquarters staff for getting the papers into print. The Editor shares the responsibility for determining the actual contents of the journal with the other members of the Editorial Board. In the past, the Chairman of the PGEC Publications Committee also served as the Editor. The time has come, however, when the duties of the Editor of the *Transactions* should be separated from the other activities of the Publications Committee, if both are to thrive.

The Professional Group on Electronic Computers is very fortunate that Ralph E. Meagher has agreed to take over as Editor, for he is well qualified for such a job. As many readers already know, he is Research Professor of Physics and Chief Engineer for the Digital Computer Laboratory at the University of Illinois. Prof. Meagher received the B.S. degree from the University of Chicago, an M.S. from the Massachusetts Institute of Technology, and a Ph.D. from the University of Illinois. Like many another computer pioneer, he worked on the development of radar during the war at the MIT Radiation Laboratory. At the University of Illinois Prof. Meagher was in charge of the engineering work on both the ORDVAC and the ILLIAC computers. He is currently directing research work in transistor circuits for computers and high-speed memories. A further qualification should be that Prof. Meagher is a member of the Board of Editors of the *Review of Scientific Instruments*.

This issue of the *PGEC Transactions* is marked by another change. The text is now printed by letterpress, rather than by offset printing from typed masters. The improved appearance is made possible because the circulation has grown to the point where the letterpress process becomes more economical. It is quite a healthy growth for a journal less than two years old, and it reflects the continuing development of the computer field. The current issue looks like a good start for a new Editor. He has our best wishes and the assurance of full support from the PGEC.

W. Buchholz
Chairman, Publications Committee

A Permanent High Speed Store for Use with Digital Computers

R. D. RYAN*

Summary—**A new type of high speed store is proposed for an electronic digital computer using interpretive program techniques. The store is based on the flying spot technique used in television signal generation. The information in the store may be read rapidly but is nonerasable. This store has the advantages of high storage density, good reliability and nonvolatility of information.**

Introduction

AN IMPORTANT element of electronic digital computers is the high speed store which holds the program instructions and data necessary for carrying out the desired computation. The requirements which this store has to meet are:

1. Storage capacity of between 1,000 and 10,000 sixteen binary digit numbers, or their equivalent.
2. Access time (for reading, writing, and erasing) of less than one millisecond and preferably as low as twenty microseconds.
3. A high degree of reliability.

Other desirable, although not essential, requirements are that of:

4. Nonvolatility, i.e. no loss of information stored when the power is switched off; and
5. Compactness.

Devices presently used to meet these requirements are:

(a) Mercury delay lines.
(b) Cathode-ray storage tubes.
(c) Magnetic core matrixes.

A defect common to all these devices is the relatively low storage density possible; to satisfy requirement (1) a large amount of equipment is needed. All of these storage devices are capable of having data read into them as rapidly as it can be read out; the store is nonpermanent and may be changed as often as may be required during the progress of a computation. While it is obvious that this property of erasability is essential for some part of the high speed store, it is not the case, as has been implicitly assumed, that the *whole* of the store must be erasable. In fact the observation of the progress of a number of programs on the CSIRO computer[1] has shown that only a very small part of the data in the store is changed during the computation. The registers associated with the arithmetic unit do, of course, change their contents continually during the computation.

A study[2] of computer programs shows that the amount of variable data in the store is not likely to exceed 5 per cent of the total. Briefly this is because most of the data in the store is concerned with organizing sequences of transfers from one part of the computer to another and that these sequences are used over and over again to operate on the relatively small proportion of variable data.

On present computers each program is, in general, quite different from other programs and so although it is not necessary to change much of the high speed store during each program run, it must be changed completely—and rapidly—each time a new program is put on the computer. However, by a suitable logical design of a computer using interpretive techniques,[2] a large proportion of the high speed store may be required to hold only a number of permanent "function blocks," which, in conjunction with hyper-programs (held in a low speed backing store of the magnetic drum type) would allow the computer to perform many different programs. There would be a need for a small number (about twenty) of such permanent function blocks in order to handle all possible programs.[3]

For a machine of this type, requirement (1) is satisfied by a high speed variable storage capacity of less than 250 sixteen binary digit numbers, together with a permanent high speed store for about 1,000 such numbers. The variable store may be obtained quite satisfactorily using one of the devices (a), (b), or (c), with reasonably small amounts of equipment. It is probable that the magnetic core matrix would be the most suitable device. The permanent store must provide a high storage density and short reading time for a small number of permanent function blocks. It must be possible to change readily the function block to handle different types of program. The rest of this paper will be devoted to a discussion of the practical realization of such a permanent store.

Flying Spot Store

It is clear that if the amount of equipment in the permanent store is to be kept to a minimum, then the only device which can provide the large amount of storage required, is the cr tube. All the other devices,

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[1] M. Beard and T. Pearcey, "An electronic computer," *Jour. Sci. Instr.*, vol. 29, pp. 305–311; October, 1952.

[2] T. Pearcey, G. W. Hill, and R. D. Ryan, "The effect of interpretive techniques on functional design of computers," *Aust. Jour. Phys.* (in press).

[3] After this manuscript had been prepared, the article (mentioned as follows) appeared, in which similar conclusions were reached. W. L. Van Der Poel, "Dead programmes for a magnetic drum automatic computer," *Appl. Sci. Res.*, vol. 3, pp. 190–198; 1953.

such as diode matrixes or magnetic core matrixes, require large numbers of storage elements and, in addition, switching circuits. Only an electron beam can be switched rapidly to a multitude of storage elements by simple switch circuits.

It is proposed that the permanent high speed store take a form similar to the flying-spot scanning system used in televising slides and motion picture films.[4] The arrangement is shown in Fig. 1. Light from the screen of

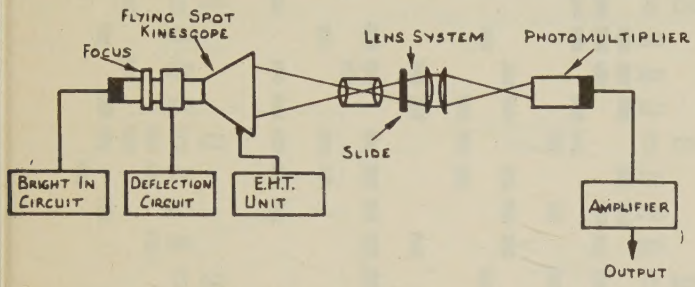

Fig. 1—Flying spot store.

the flying spot kinescope is focused so that it may be scanned across the surface of a slide, the light transmitted by the slide being focused by a second lens on to the photomultiplier tube. The slide is of the form shown in Fig. 2 (following page), with rows of black spots to represent the digits of a number. Then, as the light spot is scanned across the slide, the output from the photomultiplier will consist of a series of pulses, corresponding to the spots on the slide. Different parts of the slide may be scanned by deflecting the beam of the kinescope to the appropriate point.

The access time of this type of store is limited by the delay characteristic of the kinescope phosphor. As the beam moves from one point to another, the light intensity from the point just scanned falls quasi-exponentially, with a time-constant depending on the phosphor, and the light received by the photomultiplier is the sum of this light from the point just scanned and the light from the point at present under the beam. So, to avoid confusion between successive digit positions, the period between reading of two digits must be greater than the decay time of the phosphor. Good quality flying-spot tubes have a phosphor decay time as low as 0.5 microsecond. A digit spacing of 1.0 microsecond should therefore provide reliable operation.

Another factor to be considered in connection with the access time, is the period needed to deflect the beam of the kinescope to the point on the raster where it will scan the particular word required. Assuming the use of a magnetically deflected kinescope, the deflection time will be a function of the yoke design and the switching method used. However, in view of the television line scanning period of about 60 microseconds, it is estimated that an average deflection time of 20 microseconds should be readily obtained.

The amount of information which may be stored on each slide is ultimately limited by the size of the light spot from the kinescope, which is used to scan the slide. Each information element on the slide must be larger than the spot, if adjacent elements are to be distinguished by the scanning beam. Minimum spot size is obtained by using magnetic deflection and operating with a high gun voltage of about 25 kv. Under these conditions one can obtain a spot size as low as 0.025 mm.[5]

The resolution of the optical system and the photographically produced slide is expected to be considerably greater than that of the kinescope, viz. better than 50 lines per mm, and so may be neglected in assessing the storage capacity.

A more practical limitation on the storage capacity of the system is the problem of reliably deflecting the light spot so as to scan a particular part of the slide. To solve this problem it is necessary firstly to maintain exact registration between the resting or zero deflection position of the kinescope beam and slide, and secondly to deflect accurately the beam to a chosen point on the screen.

Registration may be maintained by mounting the components of the system on a vibration-free optical bench, and by careful regulation of the EHT, focusing and deflection units. Initial registration may be obtained by locating accurately the slide within a holder attached to the optical bench, together with a fine adjustment of the holder position relative to the kinescope.

While it might be possible to deflect the beam to a selected point by means of a deflection circuit, which provides a series of accurately defined deflection coil currents in a similar manner to the method presently used in electrostatic storage tubes, it is considered that the larger number of storage locations, within a single tube, would render this method cumbersome and unreliable. It is suggested that a better method would be to provide a co-ordinate grid of spots on the slide as shown in Fig. 2. Then, to deflect the beam to the selected point, it is first deflected along the x direction. The movement of the beam past the co-ordinate grid spots is indicated by the output of the photomultiplier, until the required x co-ordinate point is reached, whereupon the x deflection current is held constant. The beam is then deflected in the y direction in a similar fashion, and finally the beam is deflected again in the x direction so as to scan the selected data on the slide. The y co-ordinate grid spots are divided into three groups as shown in Fig. 2 so as to allow a more rapid scan in this direction. The beam is first scanned rapidly along the column with

[4] While this paper was in the manuscript stage, the author's attention was drawn to another discussion of such a system by G. W. King, G. W. Brown, and L. N. Ridenour, "Photographic techniques for information storage," PROC. I.R.E., vol. 41, pp. 1421–1428; October, 1953. It is pointed out that the problem of deflecting accurately the flying spot to a given point on the slide may make the system impracticable. The system proposed in this paper overcomes this problem by the use of a co-ordinate grid of spots on the slide.

[5] F. Roberts and J. Z. Young, "The flying spot microscope," *Proc. I.E.E.*, part IIIA, vol. 99, p. 750; 1952.

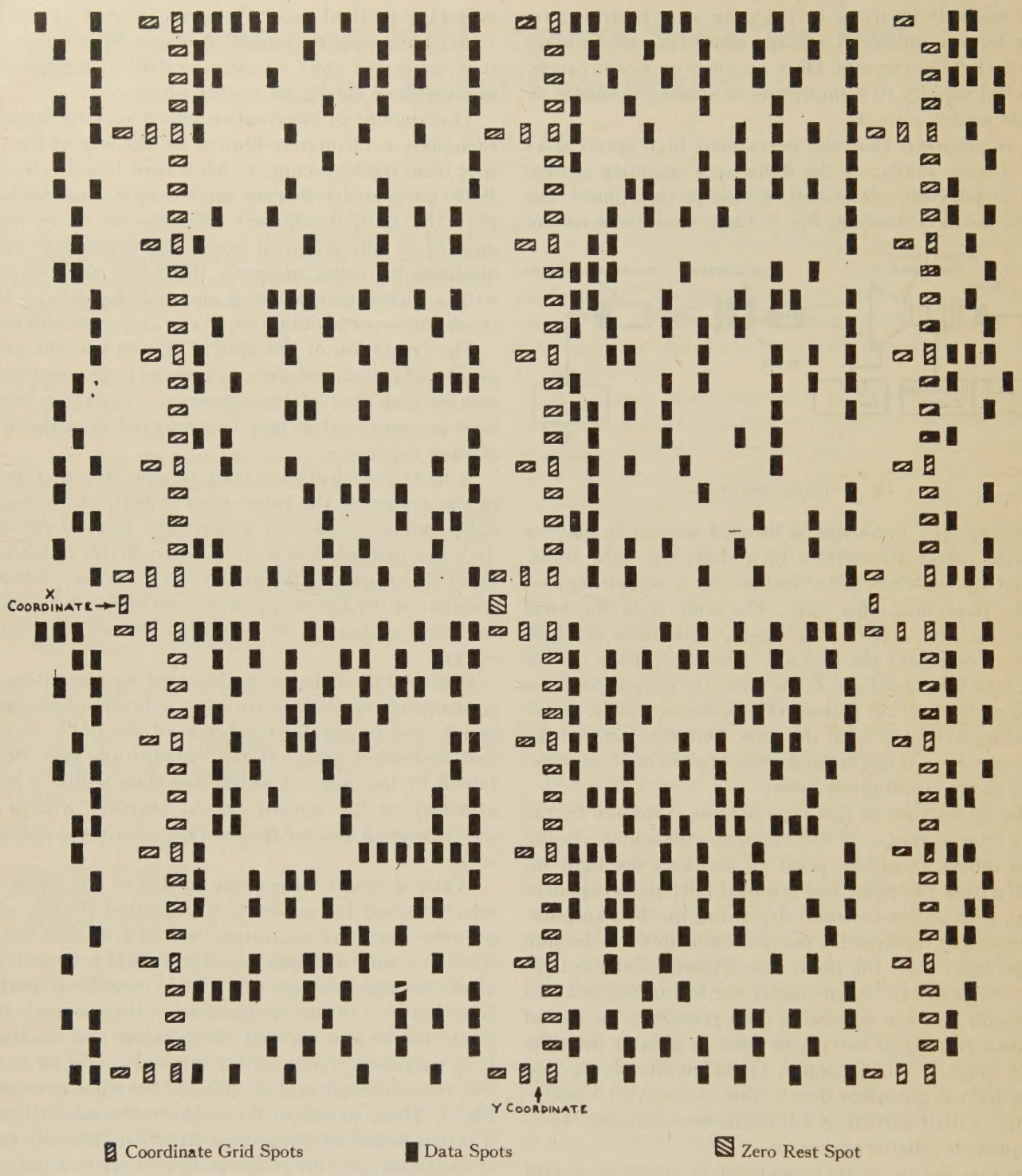

Fig. 2—Part of slide pattern.

widely spaced co-ordinate spots until the selected spot is reached, then shifted in the x direction and scanned less rapidly along the adjacent y column and finally after a second X shift, along the column of most finely divided Y co-ordinate spots. The waveforms during this selection are indicated in Fig. 3 on the opposite page. A gating circuit could be used to separate the data pulses from the co-ordinate pulses in the photomultiplier output.

The advantages of this selection method are its simplicity, as compared with an accurate deflection circuit; its independence of variations in the deflection characteristics of the kinescope and of small distortions in the slide pattern; and its expected reliability. It also simplifies the deflection circuit and yoke design, since there are no stringent linearity requirements to be met. In designing the deflection yokes, attention may be concentrated on obtaining a rapid scan and maintaining a well-focused spot over the scanned area.

Assuming this method of selection, it is possible to estimate the amount of data which may be stored within one such unit. With a slide layout as indicated in Fig. 2, and a spot size of 0.15 mm×0.3 mm. then 1,024 sixteen binary digit numbers, together with the co-ordinate grid spots, would occupy a slide area of 5.8 cm×5.0 cm. With unity magnification in the projection lens, this would make the slide spot six scanning-spot diameters wide and twelve spot diameters long. This would provide a margin of safety in guarding against erroneous reading of spots.

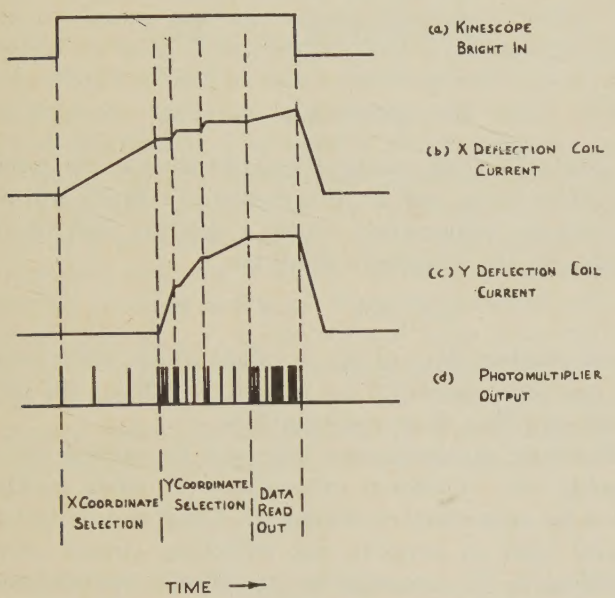

Fig. 3—Deflection waveforms.

The slide would be prepared by photographing a large scale drawing of the desired pattern, and then reducing it to slide size. It would be necessary to produce only a small number of such slides. On the slide the spots shown in Fig. 2 would actually be transparent, while the rest of the slide would be opaque. Thus, in scanning the slide, light will pass from the kinescope to the photomultiplier, only through those points corresponding to the spots on the slide scanned by the beam, and not from intermediate points between spots. This should improve the signal-to-noise ratio, by reducing to a minimum the background light due to the longer decay components of the phospor light output. It should be noted that in this storage application of the flying spot technique, in contrast with its use in television, there is no need for half-tone reproduction, but only for the detection of presence or absence of a transparent spot on the slide.

As indicated in Fig. 3(a), the kinescope beam would be switched on only during the x and y co-ordinate selection and data reading periods, and not during other periods of the computer operation. This should prolong the operating life of the kinescope, and simplify the EHT unit, in view of the small average beam current. It should also eliminate any possibility of fatigue effects on the output pulse amplitude of the photomultiplier.

If a storage capacity greater than 1,024 numbers is required, it would be a simple matter to operate a number of units in parallel, using common EHT deflection and amplifier units, and with a selection circuit for switching on the beam in the desired kinescope.

The use of a slide provides the maximum storage density, but renders more difficult the changing of the information stored. If a lower storage density can be tolerated, it would be feasible to use film in place of the slide, with the added facility for rapidly changing the information. Such changes should be relatively infrequent, occurring only when a new program is placed on the computer. Another simplification, which might be acceptable in some applications, would be to place the slide directly in contact with the face of the kinescope, and so dispense with the optical system.

Conclusion

The proposed flying spot store would satisfy the requirements for a permanent computer store. Its principal advantage is the high storage density possible, which should result in a substantial reduction in the amount of equipment required in the computer store. This, in turn, should considerably lower the cost of a computer. Another important factor is that the system uses standard commercial components, which are readily available. This, together with the small amount of equipment used, should provide a high degree of reliability. The system is also nonvolatile.

While the permanent type of store is most suitable for a computer specially designed to use interpretive techniques, it might also be used with existing computers with only slight modifications.

Application of Boolean Algebra to Switching Circuit Design and to Error Detection

D. E. MULLER*

Summary—A solution is sought to the general problem of simplifying switching circuits that have more than one output. The mathematical treatment of the problem applies only to circuits that may be represented by "polynomials" in Boolean algebra. It is shown that certain parts of the multiple output problem for such circuits may be reduced to a single output problem whose inputs are equal in number to the sum of the numbers of inputs and outputs in the original problem. A particularly simple reduction may be effected in the case of two outputs.

Various techniques are described for simplifying Boolean expressions, called "+ polynomials," in which the operation "exclusive or" appears between terms. The methods described are particularly suitable for use with an automatic computer, and have been tested on the Illiac.

An unexpected metric relationship is shown to exist between the members of certain classes of "+ polynomials" called "nets." This relationship may be used for constructing error-detecting codes, provided the number of bits in the code is a power of two.

FOLLOWING the work of Shannon,[1] design of switching circuits has leaned heavily upon logical algebra, and systematic methods have been developed by Burkhart, Kalin, Aiken, Quine,[2,3] and others for reducing polynomial expressions in logical algebra. Much of the effectiveness of the application of these techniques has depended on the skill of the designer and upon the amount of time he is willing to spend in the manipulation of algebraic expressions which are obtained after having applied systematic reduction procedures. This has been especially true in the frequently encountered case in which more than one output is required from a particular circuit. Here, systematic methods for treating the single output circuit will be extended to the multiple output case.

Multiple Output Circuits

A switching circuit will be defined as a circuit in which voltage (or current) at any point in the circuit may take either of two possible values. These values may be arbitrarily described by the symbols 0 and 1. Such a circuit will be assumed to have p points $X^1, X^2, X^3, \cdots, X^p$ at which input voltages will be applied and q other points $Z^1, Z^2, Z^3, \cdots, Z^q$ from which outputs may be taken. It will be further assumed that all voltages in the circuit will be uniquely determined by the combined effect of the p inputs. If each of the q outputs is specified for each admissible combination of values at the p inputs, then the logical specifications for the circuit have been completely given and each output may be expressed as a logical function of the inputs

$$\begin{aligned} Z^1 &= Z^1(X^1, X^2, \cdots, X^p) \\ Z^2 &= Z^2(X^1, X^2, \cdots, X^p) \\ &\cdots\cdots\cdots\cdots \\ Z^q &= Z^q(X^1, X^2, \cdots, X^p). \end{aligned} \tag{1}$$

In general, certain combinations of values at the inputs will never occur, and for this reason the inputs will not be entirely independent. Such a relation will be expressed by the subsidiary condition

$$g(X^1, X^2, \cdots, X^p) = 0. \tag{2}$$

Those combinations of input values which never occur are just those for which $g = 1$. Hence condition (2) completely specifies those combinations.

Algebraic manipulations may now be carried out to simplify the functional expressions (1) while making use of the subsidiary condition (2). These manipulations should tend to simplify the switching circuit corresponding to (1) according to prescribed criteria of simplicity, while maintaining the logical specifications for the circuits. Such manipulations, if carried out empirically, may be quite difficult and tedious. Often it is necessary to expand the functions Z^i so as to make them more complex before they can be simplified later. Systematic methods have therefore been developed to relieve the designer of some of the tedious work involved in reducing the functions Z^i.

A function Z^i of the inputs $X^1, X^2, \cdots, X^p$ may be expressed in canonical form

$$\begin{aligned} Z^i = {} & Z_0{}^i X^p X^{p-1} \cdots X^2 X^1 \vee Z_1{}^i X^p X^{p-1} \cdots X^2 \overline{X}^1 \\ & \vee \cdots \vee Z_{2^p-1}^i \overline{X}^p \overline{X}^{p-1} \cdots \overline{X}^2 \overline{X}^1 \end{aligned} \tag{3}$$

where $\overline{X}^i$ represents the complement (or negation) of X^i and the symbol "$\vee$" represents the logical operation "or." In a particular term the inputs and their complements are connected by the logical operation "and." The coefficients $Z_j{}^i$ of the $j+1$ term is a constant having either the value 0 or 1, and serves to define the value of Z^i when the input values are such that the other factors in the $j+1$ term are all 1.

Expansion (3) is a special case of what may be called a polynomial in Boolean algebra. In a general polynomial, however, it will not be necessary for a term to depend on all inputs but it may be represented by a product of less than p of the inputs and complements of inputs. Thus $X^1 \vee \overline{X}^2 X^3$ and $\overline{X}^1 \vee X^4$ would also be re-

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[1] C. E. Shannon, "A symbolic analysis of relay and switching circuits" *Trans. A.I.E.E.*, vol. 57, pp. 713–723; 1938.

[2] "The Synthesis of Electronic Computing and Control Circuits," vol. XXVII. Annals of the Computation Laboratory of Harvard University, Harvard University Press, Cambridge, Mass.; 1951.

[3] W. V. Quine, "The problem of symplifying truth functions," *Amer. Math. Monthly*, vol. 59, p. 521; October, 1952.

garded as polynomials. A different type of polynomial may be formed if the operation "exclusive or" (designated by "+") is used between terms. Such a polynomial will be referred to as a + polynomial while the previous type will be referred to as a $\vee$ polynomial. Expansion (3) may also be written as a + polynomial since all terms in (3) are disjoint (i.e., never more than one term may equal 1) and "+" may be used to replace "$\vee$" wherever it appears, giving

$$Z^i = Z_0{}^i X^p X^{p-1} \cdots X^2 X^1 + Z_1{}^i X^p X^{p-1} \cdots X^2 \overline{X}^1 + \cdots + Z^i_{2^p-1} \overline{X}^p \overline{X}^{p-1} \cdots \overline{X}^2 \overline{X}^1. \quad (4)$$

In discussing multiple output functions, results will be valid for both + polynomials and $\vee$ polynomials and the symbol "+" will be used to refer to both operations. Furthermore, the term polynomial will mean either type of polynomial. Functions in Boolean algebra such as Z^i and g will also be expressed in polynomial form.

If a suitable reduction of the functions Z^i has been achieved in polynomial form, a set of polynomials must be specified, each one of which will be used when manufacturing certain z functions. These polynomials will be written $Mj_1, j_2, \cdots, j_q$ where j_i will have the value 0 if $Mj_1, j_2, \cdots, j_q$ is used in the construction of Z^i and the value 1 if it is not. There are 2^q-1 of these polynomials, in general, since it is not possible for j_i to be 1 for all i. In reduced form the functions Z^i will be written.

$$Z^i = \sum_{j_i=0} Mj_1, j_2, \cdots, j_q \quad (5)$$

where the sum is taken over all $Mj_1, j_2, \cdots, j_q$ for which $j_i=0$. In this sum the operation between the polynomials is either "$\vee$" or "+" depending upon whether $\vee$ polynomials or + polynomials are being used. In forming the switching circuit having outputs Z^i each of the polynomials $Mj_1, j_2, \cdots, j_q$ will be manufactured first and then combined according to (5) giving the Z^i.

The problem of reducing the switching circuit producing the outputs Z^i may now be considered in two parts:

(a) The problem of simultaneously minimizing the set of polynomials $Mj_1, j_2, \cdots, j_q$.

(b) The problem of minimizing the number of connectives between such polynomials in (5). When none of the polynomials $Mj_1, j_2, \cdots, j_q$ are zero, part (b) may be ignored, since the structure of the connectives is unalterable. On the other hand, if the number of outputs is large and the number of inputs small, part (b) tends to assume importance comparable to part (a).

Theorem 1: The problem of simultaneously minimizing the polynomials used in constructing a circuit having p inputs and q outputs may be replaced by the problem of finding a minimal polynomial to represent a certain single output circuit having $p+q$ inputs.

Proof: It is not necessary to define precisely the meaning of minimization for the purposes of this theorem since the two processes are merely to be shown to be equivalent.

The imaginary single output circuit described in the above theorem is assumed to use q inputs $y^1, y^2, \cdots, y^q$ in addition to inputs $X^1, X^2, \cdots, X^p$ which are used in the multiple output circuit. The single output F of the imaginary circuit is defined as

$$F = \sum_{i=1}^{q} \bar{y}^i Z^i(X^1, X^2, \cdots, X^p). \quad (6)$$

Just as the inputs $X^1, X^2, \cdots, X^p$ are assumed to be restricted by the condition $g(X^1, X^2, \cdots, X^p)=0$ the artificial inputs y^i will be restricted by the conditions:

$$\bar{y}^i \bar{y}^j = 0 \quad \text{when} \quad i \neq j$$
$$y^1 y^2 \cdots y^q = 0. \quad (7)$$

In order to express all of these conditions as a single condition they may be added, giving

$$g(X^1, X^2, \cdots, X^p) \vee y^1 y^2 \cdots y^q \vee \sum_{i \neq j} \bar{y}^i \bar{y}^j = 0. \quad (8)$$

The sum used in this last expression is understood to use the "$\vee$" operation while all other sums in this proof represent either "$\vee$" or "+" depending upon which type of polynomial is being considered.

If F as defined by (6) is minimized subject to condition (8) it will be represented as a polynomial P. From (7) it may be shown that

$$\bar{y}^i = y^1 y^2 \cdots y^{i-1} y^{i+1} \cdots y^q \quad (9)$$

and each $\bar{y}^i$ appearing in P may be replaced accordingly. After this has been done the resulting polynomial may be written.

$$F = P \equiv \sum (y^1)^{j_1} (y^2)^{j_2} \cdots (y^q)^{j_q} Mj_1, j_2, \cdots, j_q \quad (10)$$

where $Mj_1, j_2, \cdots, j_q$ is a polynomial involving $X^1, X^2, \cdots, X^p$ and the notation $(y^i)^{j_i}$ is defined by

$$(y^i)^{j_i} = 1 \quad \text{if} \quad j_i = 0$$
$$(y^i)^{j_i} = y^i \quad \text{if} \quad j_i = 1.$$

The sum in expression (10) is taken over the 2^q-1 combinations of values of the j_i in which not all of them are 1.

It now remains to identify the $Mj_1, j_2, \cdots, j_q$ in (10) with the $Mj_1, j_2, \cdots, j_q$ in (5). From (6) and (7) it may be seen that if $\bar{y}^i$ assumes the value 1 relation (6) will become $F=Z^i$. Eq. (10) then turns into (5) since terms in (10) containing y^i vanish. If (5) have not been minimized by this process then a more reduced set of $Mj_1, j_2, \cdots, j_q$ exists satisfying (5). These equations may be substituted in (6) and using (7) may be manipulated into form (10) thus giving a more reduced version of (10). Since (10) was assumed to be minimal this contradicts the hypothesis and the theorem is proved.

Eqs. (5) now represent the multiple output circuit made up of minimal polynomials $Mj_1, j_2, \cdots, j_q$.

Theorem 1 specializes in a convenient fashion when $q=2$, and Theorem 2 expresses this special case. Eqs. (7) then become

$$\bar{y}^1 \bar{y}^2 = 0, \qquad y^1 y^2 = 0.$$

Both of these equations will be automatically satisfied if the single condition $\bar{y}^2 = y^1$ is used. y^2 therefore may be eliminated by this equation and no subsidiary conditions are required.

Theorem 2: The problem of minimizing a two output circuit having p inputs, which is to be expressed in polynomial form, may be replaced by the problem of minimizing a single output circuit having $p+1$ inputs.

Equations may be specialized as follows:

$$Z^1 = M_{0,1} + M_{0,0}$$
$$Z^2 = M_{1,0} + M_{0,0}, \tag{5'}$$
$$F = \bar{y}^1 Z^1 + y^1 Z^2, \tag{6'}$$
$$g(X^1, X^2, \cdots, X^p) = 0, \tag{8'}$$
$$F = P \equiv \bar{y}^1 M_{0,1} + y^1 M_{1,0} + M_{0,0}. \tag{10'}$$

In (6') y^1 was substituted for $\bar{y}^2$ of (6), and in (10') $\bar{y}^1$ was substituted for y^2. In this way (7) becomes unnecessary.

By way of example the set of equations

$$Z^1 = X^3X^2X^1 + X^3\overline{X}^2\overline{X}^1 + \overline{X}^3X^2\overline{X}^1 + \overline{X}^3\overline{X}^2X^1$$
$$Z^2 = X^3X^2X^1 + X^3X^2\overline{X}^1 + X^3\overline{X}^2X^1 + \overline{X}^3X^2X^1$$

may be used with no subsidiary conditions. These equations represent a single stage binary adder where Z^1 is the output and Z^2 is the carry. Eq. (6') becomes

$$F = \bar{y}^1X^3X^2X^1 + \bar{y}^1X^3\overline{X}^2\overline{X}^1 + \bar{y}^1\overline{X}^3X^2\overline{X}^1 + \bar{y}^1\overline{X}^3\overline{X}^2X^1 + y^1X^3X^2X^1 + y^1X^3X^2\overline{X}^1 + y^1X^3\overline{X}^2X^1 + y^1\overline{X}^3X^2X^1.$$

Again no subsidiary conditions are to be used. Using + polynomial reduction techniques, to be described in the next section, this polynomial may be reduced to

$$F = \bar{y}^1\overline{X}^3\overline{X}^2 + \bar{y}^1\overline{X}^1 + y^1X^3X^1 + y^1X^2X^1 + X^3X^2.$$

This gives

$$M_{0,1} \equiv \overline{X}^3\overline{X}^2 + \overline{X}^1$$
$$M_{1,0} \equiv X^3X^1 + X^2X^1$$
$$M_{0,0} \equiv X^3X^2$$

to complete the construction.

The multiple output circuit is represented by

$$Z^1 = \overline{X}^3\overline{X}^2 + \overline{X}^1 + X^3X^2$$
$$Z^2 = X^3X^1 + X^2X^1 + X^3X^2.$$

These expressions are not necessarily the simplest forms for Z^1 and Z^2. Further reduction, by replacing "+" with "$\vee$" and by factoring, are outside the realm of the present discussion since the resulting expressions would then no longer be polynomials.

Reduction of + Polynomials

Reduction of $\vee$ polynomials has been completely analyzed by Quine[3] and by Burkhart, Kalin, and Aiken.[2] Extension of these methods to include the possibility of subsidiary conditions has been carried out by I. S. Reed.[4] Applying these methods to theorem 1 permits multiple output circuits to be treated also.

Circuit reduction by use of methods involving + polynomials presents an alternative process which usually yields considerably different results from those involving $\vee$ polynomials. By way of review, the important properties of the operation "+" are:

$$\begin{aligned}
&\text{i)} && a + b = a\bar{b} \vee \bar{a}b \\
&\text{ii)} && a + b = b + a \\
&\text{iii)} && a + (b + c) = (a + b) + c \\
&\text{iv)} && a(b + c) = ab + ac \\
&\text{v)} && a + a = 0 \\
&\text{vi)} && a + \bar{a} = 1.
\end{aligned} \tag{11}$$

If property (i) is taken as a definition the other properties may be directly deduced. Because of rule (v), it is evident that one need never retain duplicate terms in a polynomial. For this reason it will be assumed that duplicate terms are always to be combined in any polynomial representation. Operations may be performed upon polynomials which leave them equal to the same Boolean function but change their form. Two polynomials, P_1 and P_2 will be regarded as equivalent only if they are termwise equivalent. Such a relation will be written $P_1 \equiv P_2$ while $P_1 = P_2$ will be taken to mean that the two polynomials equal the same Boolean function, but are not necessarily equivalent. The symbol $P_1 + P_2$ will represent a polynomial containing the terms of both P_1 and P_2 with the exception that duplicate terms are combined according to (v). P_1P_2 will represent the expanded product of the two polynomials and $P_1 \cdot P_2$ will represent a polynomial having only those terms which are common to P_1 and P_2.

A general operator R_j which may be used to alter the form of a + polynomial without changing it functionally is defined by the relation

$$R_jP \equiv P + X^jM + \overline{X}^jM + M$$

where M is a + polynomial which depends on R_j and may or may not depend on P. If M is independent of P the operator R_j is its own inverse since $R_jR_jP \equiv P$. Special operators of this type may be formed in various ways. Four operators of type R_j may be defined by writing:

$$P \equiv X^jM_0 + \overline{X}^jM_1 + M_2$$

where M_0, M_1 and M_2 are polynomials which are independent of X^j. They are:

$$A_jP \equiv P + X^jM_2 + \overline{X}^jM_2 + M_2$$
$$B_jP \equiv P + X^jM_1 + \overline{X}^jM_1 + M_1$$
$$C_jP \equiv P + X^jM_0 + \overline{X}^jM_0 + M_0$$
$$D_jP \equiv P + X^j(M_0 + M_1 + M_2) + \overline{X}^j(M_0 + M_1 + M_2) + (M_0 + M_1 + M_2).$$

The symbol Q_j will be used to denote any one of these four operators, and can be shown to possess the algebraic properties

[4] Technical Memo No. 23, Lincoln Lab., M.I.T.

1) $$Q_j(P_1 + P_2) \equiv Q_jP_1 + Q_jP_2$$

2) $$Q_jQ_kP \equiv Q_kQ_jP$$

3) $$Q_jR_jP \equiv Q_jP \quad (\text{any } R_j).$$

Theorem 3: The operator $A_pA_{p-1} \cdots A_1$ reduces a polynomial P to its canonical form (4).

Proof: A_jP is a polynomial in which each term contains either X^j or $\overline{X}^j$. To see this one may write

$$\begin{aligned} A_jP &\equiv P + X^jM_2 + \overline{X}^jM_2 + M_2 \\ &\equiv X^jM_0 + \overline{X}^jM_1 + M_2 + X^jM_2 + \overline{X}^jM_2 + M_2 \\ &\equiv X^j(M_0 + M_2) + \overline{X}^j(M_1 + M_2). \end{aligned}$$

If all terms in the polynomial P contain either X^k or $\overline{X}^k$, then A_jP also possesses this property since no terms containing neither X^k nor $\overline{X}^k$ are introduced. Hence every term of $A_pA_{p-1} \cdots A_1P$ contains either each input or its complement. Therefore $A_pA_{p-1} \cdots A_1P$ has the form of (4) which is a unique canonical form for each function. Henceforth the expression $A_pA_{p-1} \cdots A_1$ will be abbreviated A.

Theorem 4: If $P_1 = P_2$ then it is possible to transform P_1 into P_2 by p operations of the general type R_j.

Proof: If P_3 represents the canonical form of P_1 and P_2, the relations $AP_1 \equiv P_3$ and $AP_2 \equiv P_3$ are satisfied. The polynomials M_2 in the expression $A_jP \equiv P + X^jM_2 + \overline{X}^jM_2 + M_2$ may now be regarded as constants which do not depend on P since they are defined by the relations $AP_1 \equiv P_3$ and $AP_2 \equiv P_3$. The resulting operators may no longer be regarded as of the type A_j since the M's involved are constants. These operators will be written $S_pS_{p-1} \cdots S_1P_1 \equiv P_3$ and $T_pT_{p-1} \cdots T_1P_2 \equiv P_3$.

The operator S_j has the same effect as A_j when used in this equation but when applied to a different polynomial it would not have the same effect since the polynomial M_2 would be altered in the case of A_j and not in the case of S_j.

Thus if

$$P \equiv X^jM_0 + \overline{X}^jM_1 + M_2$$

and

$$P' \equiv X^jM_0' + \overline{X}^jM_1' + M_2'$$

then

$$A_jP \equiv P + X^jM_2 + \overline{X}^jM_2 + M_2$$

and

$$S_jP \equiv P + X^jM_2 + \overline{X}^jM_2 + M_2$$

but

$$A_jP' \equiv P' + X^jM_2' + \overline{X}^jM_2' + M_2'$$

while

$$S_jP' \equiv P' + X^jM_2 + \overline{X}^jM_2 + M_2.$$

Since operators using constant M commute and are their own inverses it is evident that

$$P_3 \equiv S_1S_2 \cdots S_pP_1$$

and

$$\begin{aligned} P_2 &\equiv T_pT_{p-1} \cdots T_1S_1S_2 \cdots S_pP_1 \\ &\equiv T_pS_pT_{p-1}S_{p-1} \cdots T_1S_1P_1. \end{aligned}$$

The operator T_jS_j may, however, be regarded as a single operator since the M's involved may be added, and the theorem is proved.

From theorem 4 it may be seen that operations of the type R_j are sufficient to reduce any arbitrary polynomial P_1 to its minimal form P_2. Such a reduction is not in general possible simply because the required operations cannot usually be found without a knowledge of P_2.

If operators of type Q_j are combined, a variety of characteristic forms are obtained. Theorem 5 proves the existence of these forms.

Theorem 5: If $P_1 = P_2$ then $Q_pQ_{p-1} \cdots Q_1P_1 \equiv Q_pQ_{p-1} \cdots Q_1P_2$ where Q_j may represent different ones of the four operators A_j, B_j, C_j or D_j for each j, but must have the same meaning on the two sides of the equation.

Proof: Let $AP_1 \equiv AP_2 \equiv P_3$.
Then $Q_pQ_{p-1} \cdots Q_1P_3 \equiv Q_pQ_{p-1} \cdots Q_1A_pA_{p-1} \cdots A_1P_1 \equiv Q_pQ_{p-1} \cdots Q_1P_1$ by properties 1 and 3. Similarly, $Q_pQ_{p-1} \cdots Q_1P_3 \equiv Q_pQ_{p-1} \cdots Q_1P_2$ and hence $Q_pQ_{p-1} \cdots Q_1P_1 \equiv Q_pQ_{p-1} \cdots Q_1P_2$.

From this property the operator $Q_pQ_{p-1} \cdots Q_1$ may be said to yield a "characteristic" polynomial. Since four possible choices are available for each operator Q_j (it may be either A_j, B_j, C_j, or D_j) the number of such expansions is 4^p. A particularly symmetrical expansion of this type is the one produced by the operator $D_pD_{p-1} \cdots D_1$. Other expansions such as that produced by $B_pB_{p-1} \cdots B_1$ have singular metric properties which will be described later.

Simplification of polynomials is carried out with the help of operators of the type Q_j but principally one must rely on the mathematically less interesting operator H_j defined by

$$\begin{aligned} H_jP \equiv P &+ X^j(M_0 \cdot M_1 + M_1 \cdot M_2 + M_2 \cdot M_0) \\ &+ \overline{X}^j(M_0 \cdot M_1 + M_1 \cdot M_2 + M_2 \cdot M_0) \\ &+ (M_0 \cdot M_1 + M_1 \cdot M_2 + M_2 \cdot M_0) \end{aligned}$$

where M_0, M_1 and M_2 do not involve X_j or $\overline{X}_j$ and are defined by the relation $P \equiv X^jM_0 + \overline{X}^jM_1 + M_2$. Polynomials represented by $M_0 \cdot M_1$ etc., are defined, as before, to be those containing terms common to M_0 and M_1 etc. H_j has none of the convenient algebraic properties of the Q_j's but it tends to reduce the number of terms in the polynomial to which it is applied. If "a" represents one term in a polynomial, H_j effects the following types of simplifications.

$$\begin{aligned} H_j(X^ja + \overline{X}^ja) &\equiv a \\ H_j(X^ja + a) &\equiv \overline{X}^ja \\ H_j(\overline{X}^ja + a) &\equiv X^ja \\ H_j(X^ja + \overline{X}^ja + a) &\equiv 0. \end{aligned} \tag{12}$$

One of the most elementary types of simplifications which can be applied to a polynomial is therefore $H_pH_{p-1} \cdots H_1P$ which will be denoted by HP. Although the operator H tends to simplify the polynomial

to which it is applied, it will usually yield a result which is far more complex than that attained by more refined methods. In order to attain greater simplification than is possible merely by use of the H operator, one may expand each term by reversing one of the first three operations (12) whenever subsequent application of the H operator effects a still greater simplification. Such a process which will be called Method I may be explained, stepwise, as follows:

1) One starts with a polynomial P_1 to be simplified. It is first reduced to canonical form.

$$P_2 \equiv AP_1.$$

2) This result is simplified initially by use of H.

$$P_3 \equiv HP_2.$$

3) A simplification operator C_j' is constructed according to the definition

$$C_j'P \equiv H[\overline{X}^j\{H(M_0 + M_1)\} + \{M_0 + M_2\}].$$

Successive application of C_j' yields

$$P_4 \equiv C_p'C_{p-1}' \cdots C_1'P_3.$$

4) An operator B_j' is constructed according to the definition

$$B_j'P \equiv H[X^j(M_0 + M_1) + H(M_2 + M_1)]$$

and the final result P_5 is given by

$$P_5 \equiv B_p'B_{p-1}' \cdots B_1'P_4.$$

In this process the operators B_j' and C_j' have the effect of expanding the polynomial whenever it may be simplified later by application of the H operator.

An operator H' which is more effective than the H operator may be formed by use of a gate polynomial KP. If $P_1 \nabla P_2$ represents a polynomial having terms which are in either or both of the polynomials P_1 and P_2, then the polynomial K_jP may be defined as

$$K_jP \equiv (X^j \nabla \overline{X}^j \nabla 1)(M_0 \nabla M_1 \nabla M_2)$$

and

$$KP \equiv K_pK_{p-1} \cdots K_1P.$$

For purposes of notation let

$$KP \equiv X^jN_0 + \overline{X}^jN_1 + N_2$$

and let

$$J_j^0P \equiv P + X^j(M_0 \cdot N_1 \cdot N_2) + \overline{X}^j(M_0 \cdot N_1 \cdot N_2) + (M_0 \cdot N_1 \cdot N_2)$$

$$J_j^1P \equiv P + X^j(N_0 \cdot M_1 \cdot N_2) + \overline{X}^j(N_0 \cdot M_1 \cdot N_2) + (N_0 \cdot M_1 \cdot N_2)$$

$$J_j^2P \equiv P + X^j(N_0 \cdot N_1 \cdot M_2) + \overline{X}^j(N_0 \cdot N_1 \cdot M_2) + (N_0 \cdot N_1 \cdot M_2)$$

and let

$$G_j^0P \equiv H_{j-1}H_{j-2} \cdots H_1H_p \cdots H_{j+1}J_j^0P$$

$$G_j^1P \equiv H_{j-1}H_{j-2} \cdots H_1H_p \cdots H_{j+1}J_j^1P$$

$$G_j^2P \equiv H_{j-1}H_{j-2} \cdots H_1H_p \cdots H_{j+1}J_j^2P.$$

Then

$$G^0P \equiv G_p^0G_{p-1}^0 \cdots G_1^0P$$

$$G^1P \equiv G_p^1G_{p-1}^1 \cdots G_1^1P$$

$$G^2P \equiv G_p^2G_{p-1}^2 \cdots G_1^2P$$

and finally

$$H'P \equiv G^2G^1G^0HP.$$

Method II may now be described as Method I with H' substituted for H wherever it appears. Method II has the advantage of forming as many as two expansions provided later contractions makes this advantageous, and thus yields a more effective, but more time-consuming process.

Justification for the choice of these processes rather than others which involve expansion and later simplification is based mainly upon their efficiency in reducing randomly chosen polynomials. A set of twenty randomly chosen functions of 5 inputs was used for comparison of different processes. Taking the number of terms in the final polynomial as a convenient measure of the effectiveness of the processes, the results obtained from Method I, Method II and the simple HA operator are compared in Table I.

TABLE I

TWENTY RANDOM FUNCTIONS OF FIVE INPUTS WERE USED TO TEST THREE SIMPLIFICATION PROCESSES. THE NUMBER OF TERMS IN THE SIMPLIFIED EXPANSION IS LISTED IN EACH CASE

Using Only HA Operator	Method I	Method II
11	7	7
9	7	6
6	5	5
9	6	6
8	7	6
10	7	6
8	7	7
9	7	7
8	6	6
7	7	6
7	7	6
9	7	7
9	7	7
10	8	7
10	8	7
8	7	7
7	5	5
8	7	7
9	6	6
8	5	5

Following polynomial-type simplifications such as Methods I and II, nonsystematic manipulation may be used to further simplify the result. Two types are especially useful:

a) Between pairs of terms of the form X^ia and $\overline{X}^ib$ the operation "+" may be replaced by "$\vee$" and between triples of the form $ab+bc+ca$ one may make the same substitution. By use of skill one should attempt to make the combination of substitutions which leave the fewest "+" operations to be performed.

b) Using skill, factor the result so as to reduce the resulting expression as much as possible.

Systematic polynomial reduction processes may conveniently be carried out by the use of high speed com-

puters. Programs for the ILLIAC have been prepared to reduce $\vee$ polynomials using the Harvard method and to reduce $+$ polynomials using Methods I and II described here. As yet none of these processes have been modified to permit the inclusion of subsidiary conditions. These programs make use of an interpretive subroutine which makes it possible to manipulate polynomials conveniently in the machine. In the memory of the machine a polynomial is represented as a set of 3^p binary digits. The position of each binary digit specifies the term. If the digit is 1 it is regarded as being present in the polynomial, and if the digit is 0 it is regarded as absent. No distinction need be made between $\vee$ polynomials and $+$ polynomials. To each input is allotted a digit of a number written in the ternary system. This digit is 0, 1, or 2 according to whether the input is present, complemented, or absent. The ternary number so obtained represents the relative position of the binary digit corresponding to a term in a polynomial. Thus to the term $\overline{X}^3X^2$ corresponds the number 102 written in the ternary system. Since 0 represents $X^3X^2X^1$ it would be placed in the first relative position and $\overline{X}^3X^2$ would be represented by a 1 in the twelfth relative position.

Using the interpretive routine it is possible to extract just those digits of the polynomial $P \equiv X^iM_0 + \overline{X}^iM_1 + M_2$ corresponding to one of the M's, say X^iM_0. By shifting these digits to a new relative position it is possible to form from these extracted digits either X^iM_0, $\overline{X}^iM_0$ or M_0. Assume that $\overline{X}^iM_0$ is formed. This result may then be combined algebraically with some other polynomial P' to form $P' + \overline{X}^iM_0$, $P' \cdot \overline{X}^iM_0$ or $P' \nabla X^iM_0$. The polynomial containing all terms not in $\overline{X}^iM_0$ may also be used when performing these combinations. Such a sequence of operations as the one described will be produced by one order in the interpretive routine. By a series of such orders the operators of the simplification processes may be formed. Special control transfer orders allow repeating a process using logical input indices $1, 2, \cdots, p-1, p$ and other orders permit algebraic operations to be performed without extractions. Various "red tape" orders are also provided.

Error Detection

In the theory of error detecting codes one deals with sequences of n binary digits. Such a set "a" may be written as a vector $a = (a_0, a_1, \cdots, a_{n-1})$ where a_i may take on values 0 or 1. A metric $L(a, b)$ has been defined with respect to two such vectors "a" and "b" as the number of components in which "a" and "b" differ.[5] This metric may be shown to possess all the usual metric properties. The problem of finding an error detecting code consists of finding a set of r vectors $r^0, r^1, \cdots, r^i, \cdots, r^{t-1}$ such that $L(r^j, r^k) \geqq d$ for $j \neq k$ when one is given a number d called the order of the code.

The theory of $+$ polynomials in Boolean algebra may be applied directly, when n and d are powers of two. n and d were not assumed to be restricted in this fashion in the definition of the general problem. If $n = 2^p$ and $d = 2^m$ the solutions so obtained give $t = 2^{C_pp + C_{p-1}p + \cdots + C_mp}$ where $C_q{}^p$ is a binomial coefficient. Components "a_i" of the vector "a" may be identified with the coefficients of the terms in expansion (4), the canonical expansion of a corresponding function "a" of p inputs in Boolean algebra. Such a canonical expansion may be regarded as a polynomial P_1.

$$a = P_1 \equiv a_0X^pX^{p-1} \cdots X^1 + a_1X^pX^{p-1} \cdots \overline{X}^1 + \cdots + a_{2^p-1}\overline{X}^p\overline{X}^{p-1} \cdots \overline{X}^1. \tag{13}$$

A characteristic polynomial P_2 may be formed by successive application of the operators Bj described previously.

$$P_2 \equiv B_pB_{p-1} \cdots B_1P_1 \equiv BP_1. \tag{14}$$

By an argument similar to that given in the proof of theorem 3, it may be seen that none of the inputs appearing in the terms of P_2 are complemented. Each input therefore is either present or absent and P_2 may be written

$$P_2 \equiv g_0X^pX^{p-1} \cdots X^1 + g_1X^pX^{p-1} \cdots X^2 + \cdots + g_{2^p-1} \tag{15}$$

The coefficients $g_0, g_1, \cdots, g_{2^p-1}$ are each either 0 or 1, and depend uniquely on $a_0, a_1, \cdots, a_{2^p-1}$. It is interesting to note that the transformation of the coefficients $a_0, a_1, \cdots, a_{2^p-1}$ to $g_0, g_1, \cdots, g_{2^p-1}$ is its own inverse. This may be seen by interchanging the role of X^i and the absence of X^i or $\overline{X}^i$ in the terms.

In expression (15) it is possible to group those terms containing a given number of inputs. There may exist $C_k{}^p$ terms having k inputs but certain terms in (15) may vanish because their coefficients are zero.

Definition: A net of logical functions of order d is defined as all those functions whose expansions (as given in (15)) contain no terms having more than $p-m$ inputs, where m is defined by the relation $2^m = d$.

Theorem 6: If $r^1, r^2, \cdots, r^t$ are members of a net of order d then $L(r^i, r^j) \geqq d$ for all pairs r^i, r^j with $i \neq j$.

Proof: The theorem is proved by induction. It is true in case $p = log_2 d$, since then the functions 0 and 1 are the only net members. Assume it is true when $p = k$ for all allowable d. It will be shown to be true when $p = k+1$.

From expansion (15) it may be noted that the members of a net are closed under the operation "$+$" since no terms containing more $p-m$ inputs can be generated by adding expansions having no such terms. Thus there is an r^l in the net such that $r^i + r^j = r^l$ for every pair r^i, r^j in the net. From the definition of the operation "$+$"

$$L(r^i, r^j) = L(r^i + r^j, 0) = L(r^l, 0).$$

Thus it is only necessary to prove that $L(r^l, 0) \geqq d$ for each non-zero member of the net r^l. If r^l, a member of the net of order d, is a function of $k+1$ inputs and is expressed in the form of (15), the $(k+1)$st input may be factored out giving

$$r^l = f^1 + X^{k+1}f^2$$

f^1 and f^2 are functions of k inputs, which are not both zero. f^1 is a member of the net of order $d/2$ and f^2 is a

[5] R. W. Hamming, "Error detecting and error correcting codes," *Bell Sys. Tech. Jour.*, vol. 29, pp. 147–160; April, 1950.

member of the net of order d. Four cases must be considered:

a) If the function f^2 is zero, then $r^l = f^1$. Regarding f^1 as a function of $k+1$ inputs the function r^l may be written as a sum of disjoint parts: $r^l = \overline{X}^{k+1}f^1 + X^{k+1}f^1$. If f^1 is written in the form of expansion 13 then it may seen that the separate parts $\overline{X}^{k+1}f^1$ and $X^{k+1}f^1$ of r^l contribute independently to $L(r^l, 0)$. Since $L(\overline{X}^{k+1}f^1, 0) \geqq d/2$ and $L(X^{k+1}f^1, 0) \geqq d/2$ the result

$$L(r^l, 0) = L(\overline{X}^{k+1}f^1, 0) + L(X^{k+1}f^1, 0) \geqq d$$

follows.

b) If the function f^1 is zero, then $r^l = X^{k+1}f^2$, and

$$L(X^{k+1}f^2, 0) \geqq d.$$

c) If f^1 and f^2 are not zero, but $f^1 = f^2$ then

$$r^l = f^2 + X^{k+1}f^2 = \overline{X}^{k+1}f^2$$

and

$$L(\overline{X}^{k+1}f^2, 0) \geqq d.$$

d) If f^1 and f^2 are not zero and not equal then

$$r^l = f^1 + X^{k+1}f^2 = \overline{X}^{k+1}f^1 + X^{k+1}f^3$$

where $f^3 = f^1 + f^2$ is not zero since $f^1 \neq f^2$ and is a member of the net of order $d/2$ by closure. Hence $L(\overline{X}^{k+1}f^1, 0) \geqq d/2$ and $L(X^{k+1}f^3, 0) \geqq d/2$ giving $L(r^l, 0) \geqq d$ since as before the expansions $\overline{X}^{k+1}f^1$ and $X^{k+1}f^3$ are disjoint.

Error detecting codes of order d may be formed therefore by use of vectors whose components are the coefficients of terms in the expansion (13) of net members. The information carried in such a code depends upon the number of coefficients in expansion (15) which are not forced to be zero by the net requirement. This number is $C_p{}^p + C_{p-1}{}^p + \cdots + C_m{}^p$ so that the number of such vectors available is $2^{C_p{}^p + C_{p-1}{}^p + \cdots + C_m{}^p}$.

For convenience expansion (15) may be used for interpreting information, and expansion (13) for transmission.

It has been shown that the members[6] of the net of order d do not always give the most numerous set of functions satisfying the relation $L(r^i, r^j) \geqq d$ and including the net members. When $d = 2^p$, 2^{p-1}, 4, 2, 1 the net does always give the most numerous set. When d takes on any other allowable value it can be shown that a more numerous set always exists which includes the net members, if sufficiently large p is used.

The case $d = 8$, $p = 5$ was investigated by use of the ILLIAC. In this case it was shown that no larger set of functions than the net members exists which satisfies $L(r^i, r^j) \geqq d$, and contains all net members. Hence the first case of a more numerous set must have $p \geqq 6$.

[6] D. E. Muller, "Metric Properties of Boolean Algebra and Their Application to Switching Circuits." Internal Report No. 46, Univ. of Illinois Graduate College, Digital Computer Laboratory.

An Algebraic Theory for Use in Digital Computer Design

E. C. NELSON*

This paper is presented as a tutorial article. It was delivered at the PGEC Los Angeles Chapter in 1951 and has been used successfully to train computer design engineers in a large research and development laboratory. Since the paper has not been published before, it is being printed in the hope that it will meet the needs of our newer members for information on the important subject of logical design.

Similar material, carefully prepared for training purposes, is, no doubt, being written in other organizations. The PGEC welcomes the opportunity to review such material for possible publication among a wider audience.—*The Editor.*

Summary—**An algebraic theory of the logical operation of digital computers is developed. This theory takes into account the dynamic (time) behavior of computer processes. The computer signals and computer elements are described. Their properties which are pertinent to the logical operation of digital computers are abstracted and formulated in mathematical terms. The signals are represented by algebraic symbols, and the way they are transformed by the elements of the computer is represented in terms of algebraic operations and functions. This computer algebra is based on Boolean algebra. Time is treated as a discrete variable and a method of taking into account the time relationships in the computer processes is developed. Specific components, such as gates, flip-flops, and magnetic drums, are analyzed, and an algebraic description of their operation is obtained.**

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Introduction

THE DESIGNING of a digital computer is largely a description of the processes to be performed by the computer and the identification of the details of these processes with the performance of particular circuit elements connected in particular ways. A computer process is a process such as the adding of two numbers stored in the memory and the recording of their sum in the memory, the transfer of a number from one memory location to another, or the entry of a number (or instruction) into the computer. These processes all consist of the production of particular sequences of signals from certain primary signals—primary signals being signals

that are produced by input devices or by various signal generators in the computer. The primary signals are, during the computer processes, controlled and transformed in definite ways by the elements of the computer. The problems of computer design are the selection of computer elements and the finding of ways to connect them together so that they will control and transform the computer signals in a manner that represents the correct process.

Usually computer design is carried out by drawing block diagrams showing the circuit elements and their connections. The construction of a block diagram from a set of statements describing a computer process is often tedious, owing to the difficulty of tracing the path of the signals through the maze of circuit elements involved. An algebraic representation of computer processes has been developed in which there is a direct correspondence between the algebraic operations and the circuit elements. This algebra exhibits the various signals involved and shows how they are related to the primary signals. It applies not only to the state of a computer at a definite time but also takes account of the dynamic behavior of the computer, exhibiting the time relationships between the signals in the various parts of the computer. The translation of a verbal description of a computer process into a list of algebraic equations is usually much simpler than the direct construction of a block diagram, for the equations show more clearly the role of the various signals and their relative timing. A block diagram can be constructed from the equations in a matter of minutes.

The development of this algebraic theory of computers begins with a description of the computer signals and computer elements. Those properties of the signals and circuit elements that are pertinent to the logical operation of the computer are abstracted and formulated in mathematical terms. The signals are represented by algebraic symbols and the way they are transformed by the elements of the computer is represented in terms of algebraic operations and functions.[1]

The Computer Signals

Numbers and control instructions are represented in electronic digital computers by discrete electric signals. Each elementary signal has, in most computers, only two permitted values. This type of signal is believed to afford the most reliable operation.

In the following analysis, the voltage (with respect to some reference potential in the computer) is used as the characteristic property of the signal; i.e., the signal at each point in the computer is described in terms of the potential of that point with respect to the computer reference potential. The two permitted values of each elementary signal are two values of the voltage, say E_1 and E_2. A signal at a point in the computer is interpreted by detecting whether the voltage at that point is near E_1 or E_2.

These two values of the voltage are described mathematically by binary digits, the binary digit 1 being correlated with the higher of the voltage values, say E_2, and the binary digit 0 with the lower of the voltage values, E_1. (It may be convenient to use different values of E_1 and E_2 at different places in the computer.) Thus the computer signals are placed in direct correspondence with binary digits, 0, 1. Owing to this binary nature of the computer signals, numbers are represented in the computer in terms of binary digits; however, the pure binary form is not always used. In many cases, it is convenient to use special binary coded forms for decimal numbers; however, the following discussion is not concerned with the nature of these codes but with a mathematical representation of the logical operation of the computer on the signals.

In the dynamic operation of the computer, numbers and control instructions appear as timed sequences of binary digits. A basic time interval is selected (on the basis of the requirements on the computer operation and the capabilities of the computer components) and used in the interpretation of the signals. The boundaries of these intervals are defined by a primary timing signal, usually called the "clock signal." Each elementary time interval is a space for a binary digit and will be referred to as a binary interval. Thus a signal in the computer consists of a time-varying voltage, which varies between E_1 and E_2. If the voltage rises to the value E_2 during a binary interval, the binary digit of the signal for that interval is 1; if the voltage remains at the value E_1 during the entire interval, however, the binary digit for that interval is 0.

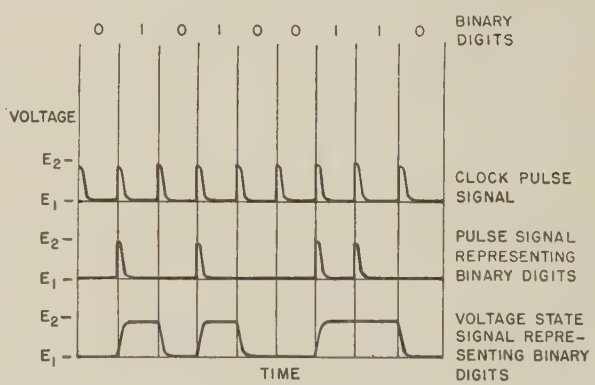

Fig. 1—Computer signal waveforms.

Two types of waveform of the voltage signals are commonly used in computers (Fig. 1). In one type, the binary digit 1 is represented by a voltage pulse; i.e., the voltage rises from E_1 to E_2 and returns to E_1 during a binary interval. In the other type, the binary digit 1

[1] Other computer algebras have been developed independently elsewhere: W. S. McCulloch and W. Pitts, "Logical Calculus of the Ideas Immanent in Nervous Activity," *Bull. Math. Biophys.*, vol. 5, p. 115, 1943; C. E. Shannon, "Synthesis of two terminal switching circuits," *Bell Sys. Tech. Jour.*, vol. 28, p. 59, 1949; H. H. Aiken and Staff of Harvard Computation Lab., "Synthesis of Electronic Computing and Control Circuits," Harvard Univ. Press, 1951—first published in Prog. Reps. Harvard Computation Lab., 1949; F. Steele and O. Eckdahl, papers presented at Rutgers Univ. meeting of Assn. for Computing Machinery, 1950; J. von Newmann, "Probalistic Logics," lectures delivered at Calif. Inst. Tech., 1952.

is represented by a voltage state (called a "pulse envelope" by some), the voltage rising to E_2 and remaining there for the rest of the binary interval. In both types, the binary digit 0 is represented by the voltage remaining at the value E_1 throughout the entire binary interval.

The signals are represented algebraically by letter symbols, such as A, B, C, Q, etc.—the signal variables. Since the signals are, for this analysis, completely described by binary digits, the signal variables take on only the values 0, 1. Time is broken up into discrete intervals, referred to in this article as "binary intervals"; hence, it is treated as a discrete variable. The computer signals at various binary intervals are represented by a signal variable with a subscript designating the interval attached; e.g., S_n represents the signal at time interval n at some specified point in the computer.

Computer Elements as Functions of Signal Variables

Definition of Functions of Signal Variables

Computer elements are devices that transform a signal (input signal) or set of signals into another signal (output signal). Such devices are shown schematically in Fig. 2. Devices represented by boxes are shown pro-

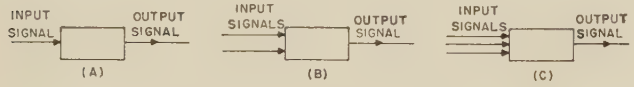

Fig. 2—Computer elements as signal-transforming devices.

ducing an output signal from (1) a single input signal in Fig. 2 (a), (2) two input signals in Fig. 2 (b), and (3) three input signals in Fig. 2 (c). In fact, the entire computer can be represented as a box with an output terminal (or terminals) to which the results of computations are delivered and input terminals to which the data to be processed are supplied. The designing of a computer consists in describing the relationship between the input and output signals in terms of elementary devices, the detailed construction of which is well known.

A mathematical description of the computer elements is obtained as follows: The relationship between the output and input signals is represented as a functional relationship between the signal variables representing those signals; i.e., the output signal variable is expressed as a function of the input signal variables. Different devices are represented by different functions. In this theory, a function is defined just as in ordinary mathematics; i.e., a function of a variable (or variables) is a rule that assigns to each value of that variable (or set of values of those variables) a unique value, the function value. Thus if A is a signal variable, a function of A, designated by $F(A)$, is a rule that assigns to each value of A a value $F(A)$. A is called the argument of the function $F(A)$.

Owing to the fact that the signal variables take on only two values, 0 and 1, the number of possible functions of one variable is very small. They can be constructed by writing down all the possible assignments of the values 0 and 1 to the values 0 and 1. These functions are shown in Table I. Two of these functions, $F^{(1)}$

TABLE I
Possible Functions of One Variable

A	$F^{(1)}(A)$	$F^{(2)}(A)$	$F^{(3)}(A)$	$F^{(4)}(A)$
0	0	0	1	1
1	0	1	0	1

and $F^{(4)}$, are trivial since they do not change at all when A changes. The function $F^{(2)}$ is equal to its argument A.

$$F^{(2)}(A) = A. \tag{1}$$

The function $F^{(3)}$ is so important in computer design that it is given a special name and notation, *complement of* A, and is denoted by a horizontal bar placed over the variable.

$$\overline{A} = F^{(3)}(A). \tag{2}$$

The complement relationship is a reciprocal one; i.e., the complement of the complement of a variable is the variable itself.

$$(\overline{\overline{A}}) = F^{(3)}(\overline{A}) = A. \tag{3}$$

Most computer processes involve functions of several variables—e.g., $F(A, B)$, $G(A, B, C)$. There are sixteen possible functions of two variables. They are presented in Table II.

TABLE II
Possible Functions of Two Variables

A	B	$F^{(1)}$	$F^{(2)}$	$F^{(3)}$	$F^{(4)}$	$F^{(5)}$	$F^{(6)}$	$F^{(7)}$	$F^{(8)}$
0	0	0	1	0	0	0	1	1	1
0	1	0	0	1	0	0	1	0	0
1	0	0	0	0	1	0	0	1	0
1	1	0	0	0	0	1	0	0	1
A	B	$F^{(9)}$	$F^{(10)}$	$F^{(11)}$	$F^{(12)}$	$F^{(13)}$	$F^{(14)}$	$F^{(15)}$	$F^{(16)}$
0	0	0	0	0	1	1	1	0	1
0	1	1	1	0	1	1	0	1	1
1	0	1	0	1	1	0	1	1	1
1	1	0	1	1	0	1	1	1	1

Boolean Algebra

Six of the functions presented in Table II can be expressed in terms of algebraic operations developed above. They are:

$$\begin{aligned} F^{(1)} &= 0 & F^{(10)} &= B \\ F^{(11)} &= A & F^{(7)} &= \overline{B} \\ F^{(6)} &= \overline{A} & F^{(16)} &= 1. \end{aligned} \tag{4}$$

Additional concepts must be used in order to express the remaining ten functions in terms of mathematical operations on the argument variables, A and B. They

can be obtained from an existing body of mathematics, Boolean algebra,[2,3] which turns out to be particularly appropriate for use in computer design, for it provides a simple mathematical description of many computer elements.

There are two basic operations in Boolean algebra. They are called addition and multiplication. (Sometimes they are referred to as "logical addition" and "logical multiplication" in order to distinguish them from the operations of addition and multiplication used in ordinary algebra. The modifier logical is used because Boolean algebra was first developed to provide a mathematical formulation of logic.)

Multiplication in Boolean algebra has the same rules as the operation of the same name in ordinary algebra. It is denoted by a dot ($\cdot$); i.e., the multiplication of the signal variables A and B is denoted by $A \cdot B$. The multiplication table is presented in Table III.

TABLE III
MULTIPLICATION TABLE FOR BOOLEAN ALGEBRA

A B	$A \cdot B$
0 0	$0 \cdot 0 = 0$
0 1	$0 \cdot 1 = 0$
1 0	$1 \cdot 0 = 0$
1 1	$1 \cdot 1 = 1$

Four of the functions in Table II can be written in terms of multiplication of A, B, and their complements $\overline{A}$, $\overline{B}$.

$$\begin{aligned} F^{(2)} &= \overline{A} \cdot \overline{B} & F^{(4)} &= A \cdot \overline{B} \\ F^{(3)} &= \overline{A} \cdot B & F^{(5)} &= A \cdot B. \end{aligned} \tag{5}$$

The rules for addition in Boolean algebra differ slightly from the rules for the operation of the same name in ordinary arithmetic. They are presented in Table IV. Addition is denoted by a plus sign ($+$); i.e., the addition of the signal variables A and B is denoted by $A+B$.[4] Only the last rule is different from the corresponding rule in ordinary arithmetic.

TABLE IV

A B	$A+B$
0 0	$0+0=0$
0 1	$0+1=1$
1 0	$1+0=1$
1 1	$1+1=1$

Four of the functions in Table II can be written in terms of addition of A, B, and their complements $\overline{A}$, $\overline{B}$.

$$\begin{aligned} F^{(12)} &= \overline{A} + \overline{B} & F^{(14)} &= A + \overline{B} \\ F^{(13)} &= \overline{A} + B & F^{(15)} &= A + B. \end{aligned} \tag{6}$$

The remaining two functions, $F^{(8)}$ and $F^{(9)}$, can be expressed in terms of a combination of the operations of addition and multiplication.

$$F^{(8)} = A \cdot B + \overline{A} \cdot \overline{B}, \quad F^{(9)} = \overline{A} \cdot B + A \cdot \overline{B}. \tag{7}$$

These elementary operations, addition and multiplication, have some important properties which are exhibited in the following identities:

$$A + \overline{A} = 1 \tag{8}$$

$$A + A = A \tag{9}$$

$$A \cdot \overline{A} = 0 \tag{10}$$

$$A \cdot A = A. \tag{11}$$

These identities are easily verified with the aid of Tables III and IV. Eqs. (8) and (10) express the fact that A and $\overline{A}$ are complementary. Eqs. (9) and (11) express the idempotent property of Boolean addition and multiplication. These operations are singular in the sense that the inverse operations of subtraction and division do not exist. The cancellation laws of ordinary arithmetic do not hold in Boolean algebra; i.e., from

$$A + B = A + C \tag{12}$$

it cannot be inferred that $B = C$ and from

$$A \cdot B = A \cdot C \tag{13}$$

it cannot be inferred that $B = C$. However, if both (12) and (13) hold simultaneously, B and C are equal.

The operations of addition, multiplication, and complementation have the following symmetry: If in an algebraic expression, each addition is replaced by a multiplication, each multiplication is replaced by an addition, and each signal variable is replaced by its complement, the resulting expression is the complement of the original expression; e.g.,

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot (B + C)} = \overline{A} + \overline{B} \cdot \overline{C}.$$

Functions of three or more variables can be expressed in terms of the algebraic operations already defined—i.e., in terms of complements, products, and sums. This assertion can be proved with the aid of a set of important elementary functions called minimal polynomials.[5] A minimal polynomial of n signal variables is a product of the n variables in which each variable or its comple-

[2] For a brief but straightforward exposition of the principles of Boolean algebra, see G. Birkhoff and S. MacLane, "Modern Algebra," The Macmillan Company, New York, N. Y., pp. 311–323; 1941.

[3] Some workers in the field, particularly H. Aiken (see reference 1), prefer to use other algebras. However, the fact that the two elementary operations of Boolean algebra can be realized in terms of simple diode circuits has led the writer to prefer it.

[4] Some books on Boolean algebra use a different notation and nomenclature. The symbols $\cup$ and $\cap$ ("cup" and "cap") are used for the two algebraic operations which are called conjunction and disjunction. It seems to the writer, however, that the notation and terminology employed in algebra is appropriate for this application. The selection of $F^{(5)}$, $F^{(15)}$, and complementation as the basic operations is not mandatory; e.g., $F^{(12)}$ could be used as the single basic operation.

[5] Birkhoff and MacLane, *op. cit.*, p. 322.

ment appears once; e.g., $A \cdot B$ and $\overline{A} \cdot B$ are minimal polynomials of two variables and $A \cdot \overline{B} \cdot C$ is a minimal polynomial of three variables. A minimal polynomial is a function that has the important property that it has the value 1 only for one assignment of its argument's values; e.g., $A \cdot B$ is 1 only for $A = 1$ and $B = 1$, $\overline{A} \cdot B$ is 1 only for $A = 0$ ($\overline{A} = 1$) and $B = 1$, $A \cdot \overline{B} \cdot C$ is 1 only for $A = 1$, $B = 0$ ($\overline{B} = 1$), and $C = 1$.

For each assignment of the argument values, there exists a minimal polynomial which has the value 1 only for that assignment. That minimal polynomial is obtained by writing the variable itself for the argument value 1 and the complement of the variable for the argument value 0. The four minimal polynomials of two variables are shown in Table V, where they are listed next to the argument value assignment for which they have the value 1. The eight minimal polynomials of three

TABLE V
MINIMAL POLYNOMIALS OF TWO VARIABLES

A	B	Minimal Polynomials
0	0	$\overline{A} \cdot \overline{B}$
0	1	$\overline{A} \cdot B$
1	0	$A \cdot \overline{B}$
1	1	$A \cdot B$

variables are shown in Table VI. There are 2^n minimal polynomials of n variables.

TABLE VI
MINIMAL POLYNOMIALS OF THREE VARIABLES

A	B	C	Minimal Polynomials
0	0	0	$\overline{A} \cdot \overline{B} \cdot \overline{C}$
0	0	1	$\overline{A} \cdot \overline{B} \cdot C$
0	1	0	$\overline{A} \cdot B \cdot \overline{C}$
1	0	0	$A \cdot \overline{B} \cdot \overline{C}$
0	1	1	$\overline{A} \cdot B \cdot C$
1	0	1	$A \cdot \overline{B} \cdot C$
1	1	0	$A \cdot B \cdot \overline{C}$
1	1	1	$A \cdot B \cdot C$

Each computer signal function has the value 1 for certain values of its argument variables and the value 0 for the remaining values of its argument variables. The function can be written in algebraic form as the sum of the minimal polynomials corresponding to those values of the argument variables for which the function value is 1. Thus, an arbitrary function of n variables can be written as:

$$F = \sum_{j=0}^{j=2^n} A_j P_j{}^n. \tag{14}$$

The symbol $P_j{}^n$ designates the 2^n minimal polynomials of n variables. The coefficients A_j are 0 or 1 depending on whether the function value is 0 or 1 for the argument values associated with $P_j{}^n$. Therefore the number of possible functions is equal to the number of ways the values 0 and 1 can be assigned to the $2^n A_j$'s. This number is 2^{2^n}. For $n = 1$, there are $2^2 = 4$ functions, as previously noted; for $n = 2$, there are $2^4 = 16$ functions; for $n = 3$, there are $2^8 = 256$ functions; etc.

Reduction Formulas

A function written as the sum of minimal polynomials is usually not in its simplest form. Such a function can be simplified by the application of reduction formulas, which can be derived from the identities (8), (9), (10), and (11).[6]

The identity (9) is particularly useful, for it permits replacement of a term in an equation by the sum of two terms each identical with it and each of which may be combined separately with other terms in the equation.

The expression $A + \overline{A} \cdot B$ can be reduced to a simpler form with the aid of the identities (8) and (9).

$$\begin{aligned} A + \overline{A} \cdot B &= A \cdot (B + \overline{B}) + \overline{A} \cdot B \\ &= A \cdot B + A \cdot \overline{B} + \overline{A} \cdot B \\ &= A \cdot B + A \cdot B + A \cdot \overline{B} + \overline{A} \cdot B \\ &= A \cdot (B + \overline{B}) + (A + \overline{A}) \cdot B = A + B. \end{aligned} \tag{15}$$

This formula, (15), is particularly useful in reducing equations.

The expression $A + A \cdot B$ also can be simplified:

$$A + A \cdot B = A \cdot (1 + B) = A. \tag{16}$$

The identity (11) is used in reducing $A \cdot (A + B)$:

$$A \cdot (A + B) = A \cdot A + A \cdot B = A + A \cdot B = A. \tag{17}$$

Another useful reduction formula is:

$$\begin{aligned} A \cdot B + A \cdot C + B \cdot \overline{C} &= A \cdot B \cdot (C + \overline{C}) + A \cdot C + B \cdot \overline{C} \\ &= A \cdot B \cdot C + A \cdot B \cdot \overline{C} + A \cdot C + B \cdot C \\ &= A \cdot C \cdot (B + 1) + B \cdot \overline{C} \cdot (A + 1) \\ &= A \cdot C + B \cdot \overline{C}. \end{aligned} \tag{18}$$

In some computer processes, certain signal combinations do not occur; e.g., in a process involving the signals A, B, and C, it may happen that the signal combination $A = 1$, $B = 1$, $C = 1$ does not occur. Then $A \cdot B \cdot C$ never has the value 1; hence for that process it may be regarded as being identically 0 and may be added to any equation used in that process. Thus the term $A \cdot B \cdot \overline{C}$ can be reduced to (in this example):

$$\begin{aligned} A \cdot B \cdot \overline{C} &= A \cdot B \cdot \overline{C} + A \cdot B \cdot C \\ &= A \cdot B \cdot (\overline{C} + C) = A \cdot B. \end{aligned} \tag{19}$$

Time Relationship of Computer Signals

In the preceding discussion of functions, the time relationship of the signals was not considered. The output signal during time interval n may be dependent on the value of the input signals during preceding time inter-

[6] H. H. Aiken, reference 1, has developed a procedure for reducing formulas that involves the use of charts called "minimization charts," because they permit the finding of the minimum form of the equation.

vals, $n-1$, $n-2$, $\cdots$, as well as on their value during time interval n. This circumstance, which implies the action of a memory element, can be taken into account in the representation of the computer element by a function of the signal variables.

The output signal during time interval n is represented by a signal variable, say C_n, and the computer element by a function, say G, of the input signals, say A_n and B_n for the case of two input signals. If the value of C_n depends only on the value of the input signals during time interval n, the relationship between C_n and A_n and B_n is written in the form:

$$C_n = G(A_n, B_n). \tag{20}$$

If the value of C_n depends on the value of A during time interval $n-1$ as well as time interval n, the relationship is written in the form:

$$C_n = G(A_n, A_{n-1}, B_n). \tag{21}$$

Thus the mathematical notation permits a description of the dependence of the output signal of a computer element on the past history of the input signals.

Mathematical Representation of Specific Computer Elements

Correspondence between Algebraic Operations and Computer Elements

Functions of signal variables are used in computer design as a mathematical representation of computer processes, which involve definite relationships between the input and output signals, in terms of functional relationships between the input and output signal variables. The functions are expressed in terms of algebraic operations on the signal variables and these algebraic operations are placed in correspondence with the action of certain basic computer elements such as gates, flip-flops, magnetic drums, etc. Once this correspondence has been established, computers can be designed by writing in algebraic form the logical description of the processes that they are to perform. The computer designed in this manner is realized by identifying each algebraic operation in the design equations with the proper computer element connected as specified by the equations.

Gates

Gates are the simplest computer element to represent algebraically, for the output signal delivered by a gate at time n is derived from input signals at the same time n. A gate has two or more inputs, which receive signals, and a single output, which delivers the gated signal.

The elementary algebraic operations of addition, $A+B$, and multiplication, $A \cdot B$, can be realized in terms of simple diode gates. The circuit of the gate for the operation $A+B$ is shown in Fig. 3. It is known as an "or" gate owing to the use of this operation in mathematical logic—the output signal variable has the value 1 if either A *or* B (*or* both) have the value 1. The input signals A and B take on the potential values E_1 and E_2 (with respect to some reference potential in the computer), E_1, the lower potential, representing the binary digit 0 and E_2 representing the binary digit 1. In Fig. 3, V_0 is a potential that is less then E_1 and R is a resistor, the resistance of which is large compared to forward resistance of the diodes. The output signal is at the potential E_2 (binary digit 1) if either A or B (or both) is at E_2 and it is at E_1 (binary digit 0) only if both A and B are at E_1; hence the output-input signal relationship corresponds to that implied by the algebraic operation $A+B$.

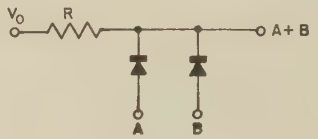

Fig. 3—Circuit of the "or" gate for the operation $A+B$.

The circuit of the gate for the operation $A \cdot B$ is shown in Fig. 4; it is known as an "and" gate, for the output signal variable has the value 1 only if both the input signals A *and* B have the value 1. The input signals A and B take on potential values E_1 and E_2 (with respect to the computer reference potential), E_1, the lower potential, representing the binary digit 0 and E_2 representing the binary digit 1. In Fig. 4, V_1 is a potential that is greater than E_2 and R is a resistor, the resistance of which is large compared to the forward resistance of the diodes. The output signal is at the potential E_2 (binary digit 1) if both A and B are at E_2 and it is at E_1 (binary digit 0) if either A or B (or both) is at E_1; hence the output-input signal relationship corresponds to that implied by the algebraic operation $A \cdot B$.

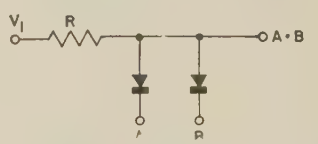

Fig. 4—Circuit for the "and" gate for the operation $A \cdot B$.

These two elementary diode gates correspond to two operations in Boolean algebra. Since an arbitrary function of signal variables can be represented in terms of these two operations on the signal variables and their complements, an arbitrary gating network can be constructed from combinations of these two types of gates.

It is important to note that this analysis describes only the logical operation of the gates. It does not describe the impedance properties or the time constants of the specific components. The questions associated with such properties must therefore be answered by a separate analysis.

The complement of a signal variable can be formed by a triode inverter, shown in Fig. 5. V_1 is the $B+$ voltage and R is the plate resistor. The input signal, A, is applied to the grid and takes on the potential values E_1 and E_2 (with respect to the computer reference potential). The lower potential, E_1, represents the binary digit 0 and is usually a few volts beyond the cutoff potential of the tube; E_2 represents the binary digit 1 and is usually equal to the cathode potential. The output signal at the plate of the tube swings between potentials E_3 and E_4 as the grid swings between E_2 and E_1.

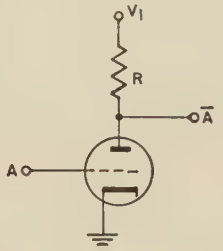

Fig. 5—Circuit of Inverter ($\overline{A}$).

The lower potential, E_3 (binary digit 0), occurs when the tube is conducting—i.e., when the grid potential is E_2 (1); and the high potential (binary digit 1), E_4 occurs when the tube is not conducting—i.e., when the grid potential is E_1 (0); hence the output-input signal relationship is that of the complement.

A pentode gate that is often used in computers is shown in Fig. 6. The two input signals, which are applied to two of the grids, operate at the potential levels E_1 or E_2 (with respect to the computer reference potential), the lower potential, E_1, representing the binary digit 0 and E_2 representing the binary digit 1. These potential levels are chosen so that the tube is conducting only if both signals A and B are at the level E_2—i.e., if both the signal variables A and B are 1. Owing to the inverting action of the tubes, the output signal, which swings between

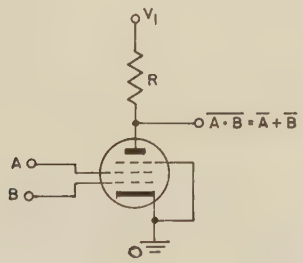

Fig. 6—Circuit of pentode gate for the operation $\overline{A \cdot B}$.

potential values E_3 (representing 0) and E_4 (representing 1), is at its high potential value, E_4 (1), unless both A and B are 1; hence, the output signal variable is the complement of $A \cdot B$ and the pentode gate is a computer element that corresponds to the algebraic operation $\overline{A \cdot B}$ $(=\overline{A}+\overline{B})$, $F^{(12)}$. This circuit could be used as the single basic gating circuit.

Two triodes connected to a common plate resistor are often used in the gate circuit shown in Fig. 7. As is the case in other tube circuits, the input signals A and B, applied to the grids of the triodes, swing between potentials E_1 (representing 0) and E_2 (representing 1).

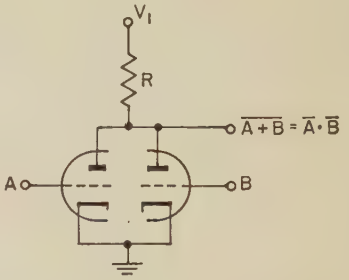

Fig. 7—Circuit for twin-triode gate for operation $\overline{A+B}$.

These potentials are chosen so that a signal having the potential E_1 cuts off the tube to which it is applied. The output signal is at its high potential value, which represents the binary digit 1, only if both A and B are at the potential E_1 (0); hence, the output signal variable is the complement of $A+B$ and the twin-triode gate is a computer element that corresponds to the algebraic operation $\overline{A+B}(=\overline{A}\cdot\overline{B})$.

Pulse-Forming Circuits

Two types of computer signals, voltage-states and pulses, were mentioned heretofore. They are distinguished by their wave form as shown in Fig. 1.

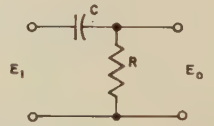

Fig. 8—Pulse-forming circuit.

A voltage-state signal can be converted into a pulse signal by means of a capacitor and resistor as shown in Fig. 8. The output signal voltage, E_0, of this circuit can be expressed in terms of the input signal voltage, E_i, and the circuit constants, R, C as shown in (22).

$$E_0(t) = \frac{1}{RC}\int_{-\infty}^{t} dt' e^{-(t-t')/RC}\frac{d}{dt'}E_i(t'). \qquad (22)$$

If RC the time constant of the circuit, is sufficiently small, the output signal is essentially the derivative of the input signal. Then a positive pulse is obtained at the output terminals when the input voltage-state signal changes from 0 to 1 and a negative pulse is obtained when the voltage-state signal changes from 1 to 0. A signal of this type which has both positive and negative pulses is often not desirable in computer circuits. Either type of pulse may be eliminated with the aid of a diode. Circuits that produce only one kind of pulse are shown

in Figs. 9 and 10. The waveforms of the signals in these circuits are shown in Fig. 11.

In the logical design of computers, it is sometimes desirable to indicate specifically this type of conversion of a voltage-state signal to a pulse signal; therefore, special symbols are used. The positive pulse conversion is designated by a prime (′) on the signal variable representing the voltage state signal; e.g., the positive pulse signal derived from the voltage-state signal A by means

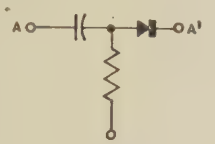

Fig. 9—Positive pulse circuit (A').

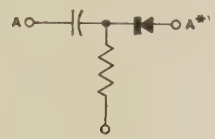

Fig. 10—Negative pulse circuit (A^*).

of the circuit of Fig. 9 is designated by A'. The negative pulse conversion is designated by an asterisk (*) on the signal variable representing the voltage-state signal; e.g., the negative pulse signal derived from the voltage state signal A by means of the circuit of Fig. 10 is designated by A^*.

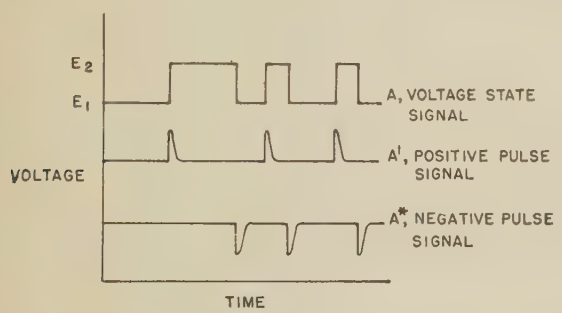

Fig. 11—Waveforms in pulse-forming circuits.

Flip-Flops

A flip-flop is a device that has two stable states. There are many kinds of flip-flops, but the one most frequently used in digital computers is a modification of the Eccles-Jordan circuit.[7] A typical circuit (Fig. 12) consists of two triodes connected together so that one is always conducting and the other nonconducting. Since the circuit is symmetric in the tubes, either tube may be the conducting one. Thus the two stable states are: (1) Tube 1 conducting, Tube 2 nonconducting; (2) Tube 1 nonconducting, Tube 2 conducting.

[7] W. H. Eccles and F. W. Jordan, "A trigger relay utilising three-electrode thermionic vacuum tubes," *Radio Rev.* vol. 1, p. 143; 1919.

This type of flip-flop has two output signals (A and B, Fig. 12), one from the plate of each tube. The signals C and D, which are applied to the grids of the tube, swing between a potential E_1 (usually a few volts beyond cut-off) representing 0 and E_2 (usually 0 volts with respect

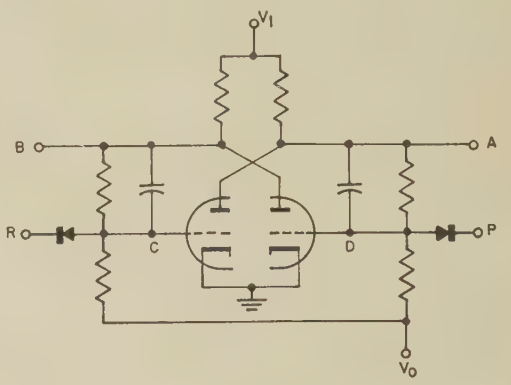

Fig. 12—Flip-flop circuit.

to the cathode) representing 1. C is obtained from B via a step-down resistor and from K. In the circuit of Fig. 12, the input signals P and R are applied through diodes connected so that the flip-flop is sensitive only to negative pulses. Thus C is at a potential E_2 (1) only if the signals B (after step-down) and R are at E_2; C is at potential E_1 if either B or R is at E_1.

$$C = B \cdot R \tag{23}$$

$$D = A \cdot P. \tag{24}$$

Owing to the inverting action of these tubes,

$$A = \overline{C} = \overline{B \cdot R} = \overline{B} + \overline{R} \tag{25}$$

$$B = \overline{D} = \overline{A \cdot P} = \overline{A} + \overline{P}. \tag{26}$$

The behavior of the flip-flop can be analyzed with the aid of (25) and (26). If the input signals have the values $P=0$, $R=1$, the values of A and B are:

$$A = \overline{B}$$

$$B = \overline{A} + 1 = 1$$

$$A = 0.$$

The zero value of P forces B into the nonconducting state, $B=1$. The signal $R=1$ does not influence A, which has its value determined by that of B. If the input signals have the values $P=1$, $R=1$, the values of A and B as given by (25) and (26) are:

$$A = \overline{B}$$

$$B = \overline{A}.$$

Hence, in this case (25) and (26) do not give definite values to A and B but only require that they are complementary. Since A and B are complementary ($A=0$, $B=1$) when $P=0$, $R=1$, their values for $P=0$, $R=1$ are consistent with the requirements of (25) and (26) when $P=1$, $R=1$. Although this analysis does not describe the dynamics of the transition, its description of the static states is consistent with the actual dynamic

behavior. If a negative pulse is applied to the P-input (and no pulse is applied simultaneously to the R-input), the flip-flop is driven into the state $A=0$, $B=1$ in which it remains after the pulse is removed.

Similarly, if a negative pulse is applied to the R-input (and no pulse is applied simultaneously to the P-input $P=1$, $R=0$), the flip-flop is driven into the state $A=1$, $B=0$ in which it remains after the pulse is removed. This property of a flip-flop, that it is set into a definite state by a pulse applied to an input and remains in that state after the pulse is removed, makes it useful as an element for storing binary information.

If negative pulses are applied simultaneously to both inputs ($P=0$, $R=0$), (25) and (26) would predict that $A=1$ and $B=1$; i.e., both tubes are cutoff. This situation would hold only if the signals $P=0$, $R=0$ are applied long enough to permit the recharging of all the capacitances in the circuit. In actual practice, short (fraction of a microsecond) pulses are used. Then the dynamic behavior of the circuit is important. Most flip-flops are designed so that when simultaneous input pulses are applied, the flip-flop changes state. The equations describing the flip-flop must be altered to include this behavior.

Since the output signals of a flip-flop are dependent on the values of the input signals in the past, the time relationship must be evident in the mathematical relationship. Let the input pulse signals designate the boundaries of the binary time intervals. Then the input pulses, P_n and R_n, can be considered as representative of the state of the rest of the computer during the time interval preceding the pulse, while the output signals of the flip-flop for the state into which it was triggered by the pulse relate to the following time interval. Thus the output signal of a flip-flop at time n is a function of its input signals at time $n-1$. This flip-flop function is designated by a special symbol Q owing to the importance of flip-flops in digital computers. The complementary relation of the two output signals is expressed by the equations:

$$\begin{aligned} A &= \overline{Q} \\ B &= Q. \end{aligned} \tag{27}$$

The dependence of Q on the input signals is presented in Table VII. An equation for Q_n can be constructed

TABLE VII
FLIP-FLOP FUNCTION Q

P_{n-1}	R_{n-1}	Q_n
0	0	$\overline{Q}_{n-1}$
0	1	1
1	0	0
1	1	Q_{n-1}

from this table.

$$\begin{aligned} Q_n &= \overline{P}_{n-1}\cdot\overline{R}_{n-1}\cdot\overline{Q}_{n-1} + \overline{P}_{n-1}\cdot R_{n-1} + P_n\cdot R_{n-1}\cdot Q_{n-1} \\ &= \overline{P}_{n-1}\cdot\overline{R}_{n-1}\cdot\overline{Q}_{n-1} + \overline{P}_{n-1}\cdot R_{n-1}\cdot(\overline{Q}_{n-1} + Q_{n-1}) \\ &\quad + P_n\cdot R_{n-1}\cdot Q_{n-1} \\ &= \overline{P}_{n-1}\cdot\overline{Q}_{n-1}\cdot(\overline{R}_{n-1} + R_{n-1}) \\ &\quad + R_{n-1}\cdot Q_{n-1}\cdot(\overline{P}_{n-1} + P_{n-1}) \\ &= \overline{P}_{n-1}\cdot\overline{Q}_{n-1} + R_{n-1}\cdot Q_{n-1}. \end{aligned} \tag{28}$$

This equation expresses the relationship between the state of the flip-flop Q_n at time n and its input signals and its state at time $n-1$. The appearance of Q's on both sides of the equation makes it a "difference" equation instead of an explicit expression for Q_n. This circumstance is due to the fact that the state of the flip-flop is dependent not only on the immediate value of the input signals but also on the values they have had in the past. It is this feature of the flip-flop that makes it very useful in computers, for it makes the device an element for storing information. Despite its implicit character, (28) is useful in designing computers; e.g., if P is set equal to $\overline{R}$ in (28), the connections for setting the signal sequence represented by the signal variable R_n into the flip-flop are exhibited.

$$\begin{aligned} Q_n &= R_{n-1}\cdot\overline{Q}_{n-1} + R_{n-1}\cdot Q_{n-1} \\ &= R_{n-1}(\overline{Q}_{n-1} + Q_{n-1}) \\ &= R_{n-1}. \end{aligned} \tag{29}$$

However, in most cases, the symbol Q_n for the output signal of the flip-flop represented by the flip-flop function Q (P, R) is sufficient to show clearly to the computer designer that a flip-flop is to be used. Thus a mathematical representation of a flip-flop is obtained in the computer algebra by defining a new function Q (P, R). This function (like the sine and cosine functions of ordinary analysis) cannot be expressed explicitly in terms of the elementary operations of addition and multiplication in its argument variables.

Other types of flip-flops, such as static magnetic flip-flops[8] or single pentode flip-flops,[9] have a somewhat different algebraic representation; however, their logical properties can be investigated in a manner similar to that used here for the conventional flip-flop.

Magnetic Drum

The magnetic drum is used as a storage device in many computers. Information is stored on it in terms of the state of magnetization of elementary magnetic regions. A magnetic drum consists of a cylinder coated with a permanent magnetic material, such as an oxide of iron. The drum is rotated at a high speed and the magnetization of the magnetic material coating the drum is scanned by heads that perform the conversion between magnetic and electric signals. Each head scans a "band" of the drum.

Just as in the case of electric signals, only two states of magnetization are used—saturation in the positive direction (with respect to some direction in the drum)

[8] An Wang and W. D. Woo, "Static magnetic storage and delay line," *Jour. Appl. Phys.*, vol. 21, p. 49; January, 1950.
[9] H. J. Reich, *Rev. Sci. Instr.* vol. 9, p. 222; 1938.

representing the binary digit 1, say, and saturation in the negative direction representing the binary digit 0. Each band of the drum is considered to be divided into tiny regions which are spaces for storing binary digits. A mathematical description of the information stored on the drum is obtained by representing it by a letter symbol, say M_n^j, which takes on the values 0 or 1 corresponding to the digit stored in digit space n of band j. This magnetic signal variable differs from the electric signal variables discussed in the preceding sections in that the subscript n is defined only for a finite number of values, the number of digit spaces in a band.

The process of recording digital information on the magnetic drum has simple logical properties. The electric signal, say A_n, from the switching circuits of the computer is amplified and sent through the magnetic recording head, which converts it into a magnetic signal that is recorded on the drum; hence, during the recording process a correspondence can be made between the electric signal variable A_n and the magnetic signal variable M_n^j. The relationship between the time index n of A_n and the space index n of M_n^j is established by identifying the binary time interval with the time required for the magnetic head to scan a magnetic binary interval on the drum and extending the domain in which the magnetic interval index is defined to include all positive and negative integers by making use of the fact that the magnetic head scans each magnetic interval once per revolution. If the number of magnetic intervals in a band of the drum is N, then the interval index $n+N$ can be defined, if n is defined, by means of the equation:

$$M_{n+N}^j = M_n^j. \tag{30}$$

If the zero point of the time index of the electric signal variable is chosen so that it coincides with the time that the magnetic interval number zero passes under the recording head, the magnetic interval index and the time index are in one to one correspondence.

With this interpretation of the relationship of the magnetic index and the time index, (30) describes band j of the magnetic drum when recording of new information on the drum is not taking place. The process of recording new information is described by the equation:

$$M_n^j = W_n^j \cdot A_n + \overline{W}_n^j \cdot M_{n-N}^j. \tag{31}$$

W_n^j, a signal variable which has the value 1 during recording and 0 otherwise, represents the signal which turns the recording amplifier on and off. (This equation does not describe the detailed dynamic behavior of the recording process. Such factors as the delays in the amplifier and the recording head must be taken into account in the design of the circuits.)

The information recorded on the magnetic drum is read by means of a magnetic head which senses the state of magnetization of the regions in the band and generates an electric signal describing them. The reading head may be the same head used in recording. In this case, the electric signal variable G_n can be expressed in terms of the magnetic signal variable M_n^j by means of the equation:

$$B_n = M_n^j. \tag{32}$$

If the head used for reading is different from the head used for recording, the equation is modified:

$$B_n = M_{n+m}^j. \tag{33}$$

m is the displacement in magnetic binary intervals of the reading head relative to the recording head.

The operation of other types of memory devices, such as acoustic delay lines, storage tubes, magnetic tapes . . . , can also be described algebraically by carrying out an analysis in a manner similar to that used for the magnetic drum.

Application Procedure

The application of this computer algebra to the design of specific digital computers is carried out as follows: The computer is defined by listing the processes it is required to perform. Each process is described by a set of statements that specify its logical properties; i.e., these statements specify the nature of the numbers or other forms of information on which the process operates and their relationship to the numbers (or other information) which the process produces. The input and output numbers (or information) are represented mathematically by signal variables and the relationships between them by functions of signal variables. Thus, the statements describing computer processes are translated into a set of algebraic equations.

The algebraic operations in the equations can be interpreted in terms of specific computer elements according to the rules given above. If computer elements not described are to be used, an algebraic representation of them can be developed in a manner similar to that used there. After the equations are initially set up from the statements describing the computer processes, those mathematical operations in them which do not represent computer elements of the kind to be used in the computer must be expressed in terms of mathematical operations representing correct computer elements. The equations may be modified further by means of reduction formulas and algebraic transformations to obtain the simplest possible mechanization.

This computer algebra has been applied in the design of several electronic digital computers.

An Improved Reading System for Magnetically Recorded Digital Data

SAMUEL LUBKIN*

Summary—In magnetic recording of pulses, whether on drum or tape, the resulting flux pattern is affected by proximity of adjacent pulses. The best defined region is that adjacent to the maximum. In reading, the signal is the derivative of the flux. In the best defined region, this is close to a straight line passing through zero when the flux is a maximum. The slope of the curve at the zero changes sign with change of pulse polarity. A new method of reading is described which examines the signal from the head for such transitions from positive to negative or reverse as indications that a positive or negative pulse had been recorded. This is done by gating the inverted signal with the delayed signal for positive pulse reading and the inverse of this for reading negative pulses. Besides providing sharply defined outputs, this method permits reading both positive and negative pulses from a single channel without interference or ambiguity. Examples are given for using this facility for checking purposes and for storage of two types of data in a common channel.

THIS paper concerns a new method of reading digital information from magnetic drums or tapes. We begin with the assumption of a two-level, return to zero type of recording on a magnetic drum in which a Binary 1 is recorded as a pulse of one magnetic polarity superimposed on a background of opposite magnetization while a Binary 0 consists merely of the unbroken background magnetization. Line A of Fig. 1

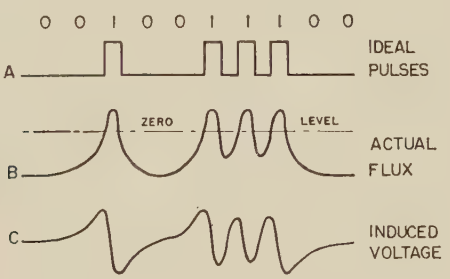

Fig. 1—Two level recording.

shows the idealized condition for the arbitrary sequence of Binary digits indicated. The actual flux recorded on the drum surface departs from the ideal because of the following factors:

1. Limitations in head and drive circuit limiting rise time.
2. Fringing of flux at magnetic head gap due to necessary mechanical clearance between head and drum and leakage.
3. Effects of recording of one pulse on adjacent pulses and backgrounds.

These factors cause the actual flux pattern to approximate Line B in Fig. 1, despite usual action to improve resolution by applying a much narrower pulse to the recording head than the ideal indicated.

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When this flux pattern passes under a reading head, the voltage induced in the head is proportional to the change of flux with some further degradation in resolution because of fringing effects in coupling to the head magnetic circuit. The induced voltage is therefore approximated by Line C of Fig. 1.

The simplest method of interpreting the induced voltage in the reading head is to amplify it and clip off all except the positive peaks. This scheme is shown in Fig. 2. It will be noted that the positive peak occurs prior to

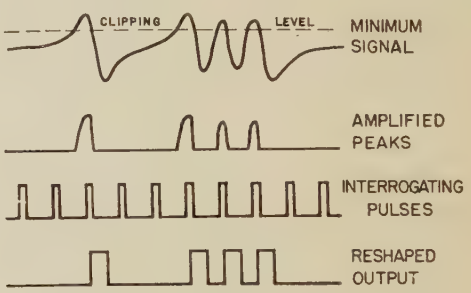

Fig. 2—Clipping of positive peaks.

the midpoint of the recorded flux. Since, as previously stated, it is customary to utilize narrow recording pulses, it becomes possible, in this system, to record in the same location as data being read and this has been proposed by various people.[1] If we assume Fig. 2 to show the lowest signal amplitude expected as a result of variations in coating and gap around a drum channel and in gain of the associated drivers and reading amplifiers during their usual life, it is possible to get amplitudes five or more times as great from the same head under most favorable conditions. Fig. 3 (opposite page) shows what may occur under these conditions. Because position of positive peak with respect to initial recording and hence clock pulses depends on adjacent pulses, and because of long "tails" on positive pulses preceded by zeros, it is found impossible to select interrogating pulse phasing so as to avoid introducing spurious output pulses if all that are actually present in the signal are to be detected.

A common way of overcoming this difficulty heretofore consisted of adding a differentiating circuit to the reading amplifiers.[2] Fig. 4 (opposite page) shows how this scheme works. The inverted differential signal is shown as clipped at zero for clarity. In actual practice, clipping is at a slightly positive value to cut out extraneous noise. The differentiation produces a well-defined

[1] J. H. McGuigan, "Combined reading and writing on a magnetic drum," PROC. I.R.E., vol. 41, pp. 1438–1444; October, 1953.

[2] Engineering Research Associates, "High Speed Computing Devices," McGraw-Hill Book Co., Inc., New York, N. Y., pp. 327–330; 1950.

positive loop per pulse which is accurately located with respect to the original recording, thereby avoiding the difficulties of the previous method. Reclocking must, however, be done at a somewhat later time. The chief disadvantage of this method is the fact that differentiation accentuates noise as compared to signal. The additional amplification needed to overcome attenuation by the differentiating circuit is, furthermore, an additional source of amplitude variation.

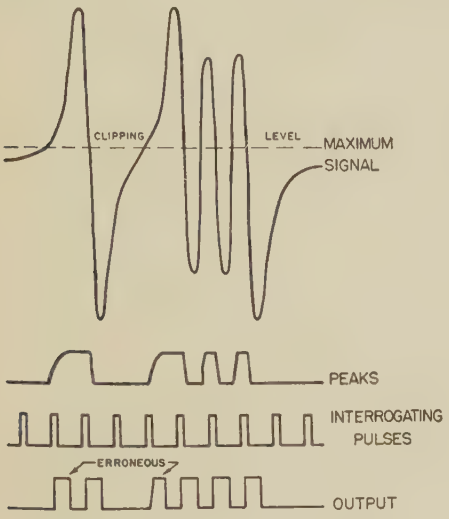

Fig. 3—Clipping of high level signals.

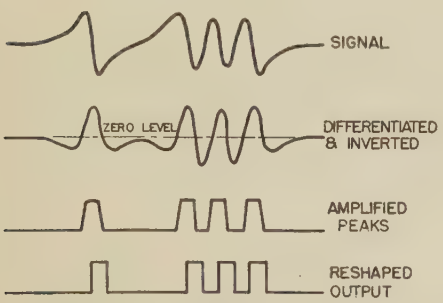

Fig. 4—Use of differentiated signal.

Fig. 5 shows the operation of a new reading method which offers advantages over both of those previously described. This may be called the dual-correlation method since it, in effect, examines the signal for correlation of both positive and negative portions with clock pulses. This method yields gating areas as sharply defined and precisely located as does the differentiation method but without the additional amplification required to make up losses in differentiating circuits and without accentuating noise as compared to signal. In fact, noise of random type is discriminated against, only that having a transition from positive to negative at standard clock positions being passed. This consists almost wholly of previous pulses not fully erased. Fig. 6 shows a logical diagram of this scheme. It uses similar components and arrangements as does the balance of the computer, making design particularly convenient. The magnitude of delay in this circuit is not critical. The greater the delay, the larger the gated signal and the less amplification needed. It is, however, desirable to avoid including the peaks in the gating since these vary in magnitude and position with pulse density and other factors to a greater degree than the slope. A good choice for the delay is, therefore, about $\frac{2}{3}$ of the time between positive peak and negative peak for the successive pulses.

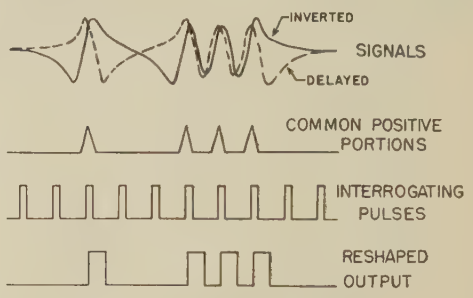

Fig. 5—Dual-correlation method.

Conditions for pulse recording on magnetic tape are somewhat different from those for similar recording on drums. This is due to many factors. On the one hand, magnetic tape is generally run in contact with the reading and writing heads which is permissible because of the lower surface speed (below 10 feet per second for tape, as high as 200 feet per second for drum) and the low number of passes on the same position over the head (perhaps 10 per hour for tape, as high as several hundred thousands per hour for drum) and the further simplicity and low cost of replacing tape when worn as compared to repair of drum. This makes resolution much better for tape as compared to drum recording. On the other hand, tape is not as well controlled in its speed or movement and thus it is not possible to utilize clock pulses to restrict pulse examination to limited regions. If tape is used in connection with several drives, channel alignment during recording may differ from that during writing. This is accentuated by possible angularity in

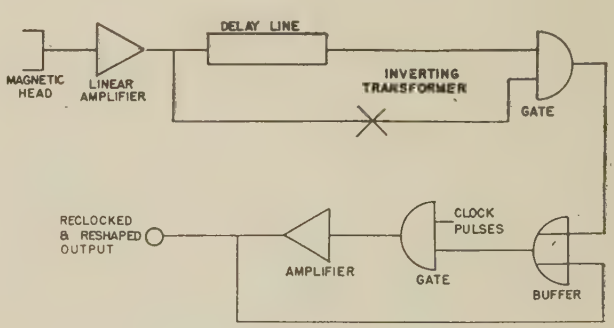

Fig. 6—Dual-correlation circuit.

running over the heads which will change channel alignment. These factors limit precision of possible control by "trigger" pulses recorded in one of the channels. For these reasons, pulses are spaced further than might ap-

pear possible from the viewpoint of resolution only. As a further consequence, pulse shape does not change materially because of adjacent pulses. The first line of Fig. 7 shows a possible head output.

Fig. 7 shows the outputs of the various signals applied to tape reading, without any clock gating. It is obvious that the simple clipping scheme gives less space between pulse outputs for correlation with other channels and conversion to synchronous signals in the computer proper. Comparison between the other two methods is similar to that made in the case of the drum.

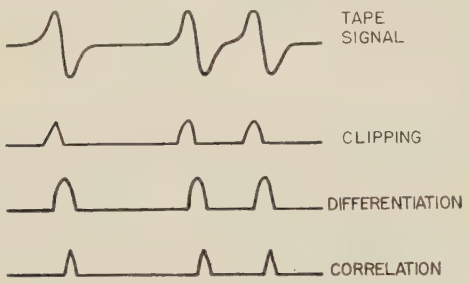

Fig. 7—Reading magnetic tape.

There is a serious difficulty in use of magnetic tape at the present time. This is the occasional presence of defects in the tape coating. It is possible that, sometime in the future, error-free tape will be produced or selected by the tape manufacturer. At the present time, however, the best tape still has a few areas in which recording is poor. When the tape is used for recording sound, such small defects are not detrimental; however, when used for recording digital information they result in loss of pulses. Several schemes have been developed to overcome this difficulty. Some manufacturers punch holes into the tape and have automatic devices which skip the portion of tape between holes as an area containing one or more defects which have been determined by an initial examination. Others have proposed cutting out defective sections and splicing the remaining portion of tape. We use a different arrangement. We pre-examine the tape for defects. In such examination, every channel in every expected pulse position is automatically recorded upon and read from. Wherever an area in any channel is found to give less than 80 per cent of normal signal, this is considered a defective area. One channel of the tape is allocated to use as a "sprocket" channel. Wherever the tape is good, a succession of pulses is recorded in this sprocket channel. Wherever a defect exists, whether in the sprocket channel or other channels in line with it, no pulses are recorded in the sprocket channel. The scheme is such that partial pulses cannot be recorded in any case. In use of the tape, the sprocket channel is never erased and recording in other channels is made only in the areas in line with sprocket pulses. Reading from the tape is similarly restricted to the same areas.

This method of pre-examination of tape not only serves to avoid tape defects in an efficient manner by skipping only the defective portions, but also provides a means for locating data in permanent allocated positions on the tape so that no amount of erasure and rerecording results in shift of data along the length of tape. Thus, in absence of sprocketing, it is possible that, because of tape speed variations and residual timing changes, one block of data which is erased and rerecorded frequently may be recorded each time slightly further along the tape; so that after, say, a hundred times of recording, it will encroach on the space allocated to the next portion of data initially recorded on the tape and, because of characteristics of the problem at hand, never erased. It has, in fact, been customary in some of the other systems to change only alternate blocks of data in order to retain a fixed set on the tape and thus prevent cumulative shifting.

Another function that can be accomplished by "sprocketing" of tape is to indicate specifically the beginning and end of each block of data. It is customary to record tape in blocks because of the greater efficiency of block transfers between tape and machine as compared to single character or word transfers in view of the finite start-stop time for the tape. For the purpose of designating blocks, it is convenient to record two different types of pulses in the sprocket channel: one to represent the location of each pulse position in the other channels, and the other to represent beginning and end of each block of data. We simplified this recording by using pulses of one polarity, say positive, for the first function and pulses of an opposite polarity throughout the region between blocks for the second function. In the case of the negative pulses, it is immaterial whether these are continuous or otherwise in the manner of use since they do not designate any individual location but serve merely to show the region between blocks. For this reason, no examination of defects is made corresponding to negative sprockets. Fig. 8 shows sprocketing on tape.

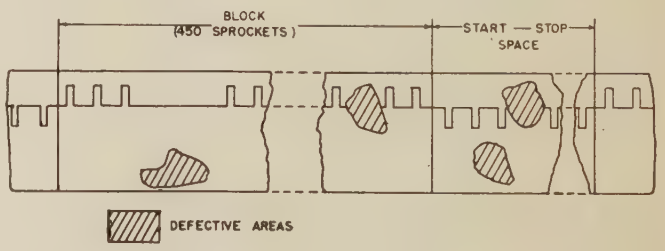

Fig. 8—Sprocketing on tape.

This use of the sprocket channel for designating block positions as well as individual pulse positions permits application of a simple check to tape reading. This is to count the number of sprockets per block. Should this number differ from the designated number (450 for the case illustrated in Fig. 8) between negative sprocket regions, an error has been made. Another useful application of the particular type of sprocketing employed concerns "hunt" along the tape. If the tape is to be moved over a great many blocks without reading or writing on it, it is merely necessary to count the number of changes from positive sprockets to negative sprockets in order to count the number of blocks passed. It is not necessary to examine the data within a block nor to count the individual sprockets.

For purposes of the sprocketing discussed above, a scheme is necessary that is capable of distinguishing between positive and negative pulses. Use is made of the fact that the pulse, in the case of tape, is small as compared to the space between pulses and that the reading system proposed in this paper can be extended to obtain unambiguous indications for both positive and negative pulses of the type mentioned. Fig. 9 shows the logic of

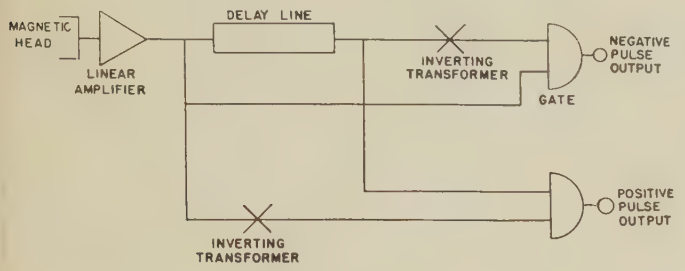

Fig. 9—Bi-direction reading circuit.

such bidirectional reading while Fig. 10 shows the operation of the system. It is to be noted that neither of the other two systems previously discussed are capable of this mode of operation; since, in each case, the resulting wave forms have areas on both sides of the axis and pulses of opposite polarity can only be distinguished on the basis of precise amplitude and/or timing examination. It is to be noted that tape has no standard timing unless mechanically sprocketed.

It is also possible to record bidirectionally on a magnetic drum if some means is provided to insure return of magnetization to zero between pulses. For tape, the zero level is insured in the case of the sprocket channel by preliminary AC erasure. This may be true for the data channels as well in certain types of application, such as handling of a complete file at a single pass, in which, instead of intermediate modifications being made, the entire file is reproduced on a new tape and the old file at a later time is re-used by erasing it completely. In the case of a drum, zero level may be achieved by AC erasure between read and write heads in recirculating type channels. In nonrecirculating type channels, it may be possible to engrave or etch the drum so as to remove magnetic material between pulses. In all these cases, it is possible to utilize positive and negative pulses which are individually read by the present scheme giving two independent outputs. By such means, an extremely

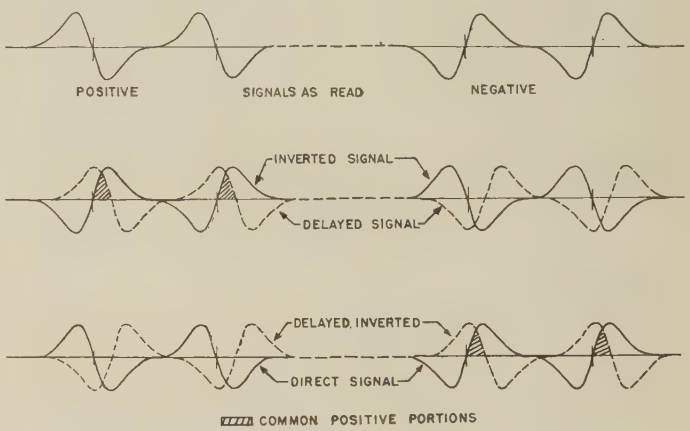

Fig. 10—Reading of positive and negative pulses.

thorough check is possible on the basis that either a positive pulse or a negative pulse—but not both—must exist in every pulse position on the drum. It would seem that such a check would be completely conclusive, except in the case of total failure of the previous recording to modify earlier data existing on the drum.

A Digital Voltage Encoder*

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Summary—**A two-channel voltage encoder having a sampling rate of 40 numbers/second in each channel has been designed for use in a data reduction system. The data are recorded on single-channel magnetic tape in the form of 10-digit binary numbers with an accuracy of ±0.1 per cent. The range of input voltage is 0 to 1 volt and may be lowered to 0 to 10 mv through the use of chopper amplifiers. This lower range of input voltage covers the voltages generated by analog transducers commonly employed to measure temperatures, pressures, flow rates, and thrusts.**

Introduction

IN RECORDING engineering data for subsequent automatic computation, it is advantageous to have these data recorded in digital form; also it is only through the use of digital methods that accuracies of 0.1 per cent may be achieved. The encoder to be described was designed for recording digitally the output of analog transducers used in rocket-motor tests. Digitized data at the encoder output are recorded on magnetic tape and are later transferred to printed tabular form or punched cards by the transcriber unit of the data-handling system.[1]

In this paper, the encoding portion of the data system is considered. Major characteristics of the encoder are as follows: There are two input channels, each with a sampling rate of 40 complete measurements per second and an input range of 0 to 1 volt. Accuracy of the encoder is ±0.1 per cent as output is described by 10 binary digits. Through the use of contact-modulated amplifiers, the input range may be lowered to 0 to 10 millivolts. This sensitivity is required for use with most input transducers.

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† Jet Propulsion Lab., Calif. Inst. of Tech., Pasadena, Calif.

[1] M. E. Frank, "Data-handling system for general instrumentation. II. Transcriber," *Proc. NEC.*, vol. 9, 1953.

Methods of Analog-to-Digital Conversion

Several methods for converting continuously varying voltages from the analog to the digital form are in common use.[2,3] Certain elements are essential in analog-to-digital converters. One such element is a reference voltage with which the input signal may be compared. Another is a comparator device which is capable of detecting coincidence between the magnitude of the input voltage and the reference voltage to the degree of accuracy desired.

Two general methods of varying reference voltage are frequently used. In one—the linear-sweep method—the reference voltage is varied continuously and smoothly as a linear function of time. In the other, incremental changes in standard voltage are made permitting successive comparisons between the standard and the unknown. When this method is used, the standard is held constant during each comparison period.

Description of Encoding Method

Any point in the interval 0 to 1 may be described by a binary number

$$\cdot a_1 a_2 a_3 \cdots a_n = a_1 \frac{1}{2^1} + a_2 \frac{1}{2^2} + a_3 \frac{1}{2^3} + \cdots + a_n \frac{1}{2^n} \cdot$$

The a values are limited to either 0 or 1. In the relay encoder the binary coefficients refer also to the position of the relay contacts in the encoder, 1 representing a closed relay and 0 an open relay. As n becomes large, the sum of the terms on the right approaches 1, when a_n equals 1. The series shown may be extended to include any number of terms; however, in a physical situation the limit of significant terms is imposed by the accuracy of measurement required or the noise level of the comparator. A point within the interval 0 to 1 volt may be described uniquely through the following sequence of operations: The binary coefficient a_1 is assumed to have the value 1, and the first term is subtracted from the unknown voltage. If the difference is positive, the value 1 is retained for a_1, whereas if the difference is negative, the a_1 is made equal to 0. Next the value of the coefficient a_2 is assumed to be 1, and the second term is subtracted from the residue of the preceding operation. The value of a_2 is determined as either 0 or 1 as before, depending on the sign of the new difference. In a similar manner, the unknown is compared with the sum of all terms of the series. The subtraction operation is realized by adding negative increments of voltage to the positive input voltages.

As these operations are performed, the binary-number equivalent of the unknown voltage is generated serially by the comparison operation. This same binary number may also be obtained in parallel form by noting the position of the relay contacts at the end of the sampling period. This parallel output provides a convenient way of displaying the binary-number output visually.

Operation of Encoder

In describing the operation of the encoder, it is convenient to follow the block diagram in Fig. 1, which shows the functional units for one channel. Trigger pulses from the clock close relays which introduce voltages into the comparator. The first relay to be closed (which corresponds to the most significant digit) adds a voltage at the comparator input which requires a positive analog input signal greater than +0.5 v to prevent release of the relay. Likewise, the second relay adds an increment requiring greater than +0.25 v to prevent its release. All the other digits are evaluated using the same scheme. It is assumed that input voltage does not change during the sampling period.

This discrimination between positive and negative sums of the series is the function of the comparator gate. Output of the comparator gate consists of reset pulses indicating 0 and blank spaces which represent 1. The complement of the reset pulses is formed and made ready for recording in the pulse-former circuit. The serial binary numbers are recorded on the tape, and the occurrence of a pulse of either polarity provides timing information for the transcriber.

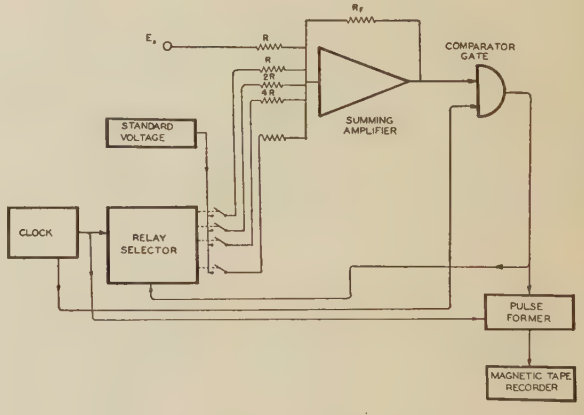

Fig. 1—Block diagram of single-channel encoder.

Since the time scale on the digitized record depends on a knowledge of the sampling rate of the encoder, an electromechanical tuning fork is used to control the frequency of the timing pulses. These timing pulses determine the closing time of the relays which introduce standard voltage increments into the summing amplifier. A second pulse which is displaced by one-half of a comparison period serves as a reset pulse when passed by the comparison gate. Thus the comparison operation is delayed until after the relay is fully closed.

The timing scheme for operation of the two-channel encoder is shown in Fig. 2. Output digits from the two channels of the encoder are interlaced in recording them on the magnetic tape. Thus the respective measurements on the two channels coincide in time. Additional

[2] M. L. Kuder, "Anodige, An Electronic Analog-to-Digital Converter," *Report No. 1117*. Washington: National Bureau of Standards, August 24, 1951.

[3] "High Speed Analog to Digital Converter," *Rev. Sci. Instr.*, vol. 22, p. 544; July, 1951.

pulses are interlaced with those of the two information channels and identify the group. At the end of a group of 30 pulses, a blank space equal to one digit period is left to separate the pulse groups representing complete samples.

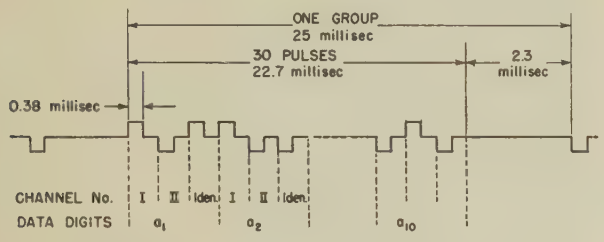

Fig. 2—Output of two-channel encoder.

For a two-channel instrument, the single-track tape recorder could have been replaced by a dual-track recorder with simplification of the transcriber circuitry. However, the single-track recorder has the advantage that the number of input channels may be increased with a minimum change in circuitry. To be useful in field recording an encoder should accept a large number of inputs and should have a simple method of data storage. For this reason a single-channel magnetic tape was used, and recordings may be made at tape speeds of 15 or 30 inches/second. Approximately 90 pulses/inch are recorded at a tape speed of 15 inches/second. This density of pulse recording is easily realized and utilizes well-known, pulse-recording techniques.[4]

Time division between channels is accomplished by a three-tube thyratron ring[5] which distributes pulses between two information channels and the identification numbers which are interspersed. All of these timing pulses for the two-channel encoder are generated by the clock circuitry. The cathode-coupled thyratron ring which acts as channel commutator operates at a rate of 1,320 pulses/second. Ring trigger pulses for the various channels are formed from the leading edge of signals at the plates of the thyratron ring. Plates of the thyratrons are connected to diode "and" gates[6] so that a reset pulse is passed to the comparator gate of the proper channel. After each 10 digits, an interval equal to the duration of 1 digit is left for readout and resetting of relays. During this period the reset pulse is blanked out so that no pulse is passed through the comparator gate. Throughout the encoder, pulse outputs which are used to drive parallel combinations of elements are shaped by blocking oscillators. The blocking oscillator provides a low-impedance output with a standard pulse amplitude and width and assures proper triggering of circuits which follow.

[4] E. S. Rich, "High Speed Pulse Recording on Magnetic Tape," *Report No. 159*. Cambridge: Servomechanisms Laboratory, Mass. Inst. of Tech., April 6, 1949.

[5] C. C. Shumard, "Ring counter circuits," *Elec. Eng.*, vol. 57, p. 209; May, 1938.

[6] T. C. Chen, "Diode coincidence and mixing circuits in digital computers," Proc. I.R.E., vol. 38, p. 511; May, 1950.

A. Comparator

Precision of this digital voltage converter is limited by the accuracy of the standard comparison voltage and also by the sensitivity and stability of the comparator device. A standard cell reference is used to maintain required accuracy of this comparison voltage, and the comparator has the following major characteristics:

1. The comparator gate passes pulses when the potential of the summing junction is negative and rejects all signals of opposite polarity regardless of amplitude.
2. Comparison sensitivity is sufficient to detect a 1-millivolt positive signal referred to the input of the summing amplifier.
3. Response time of the comparator is approximately 0.5 millisec and easily allows operation ot the sampling rate of 40 per second.
4. Offset and drift of the comparison circuit are less than 0.1 per cent of full scale, or 1 millivolt referred to the input. The comparator device which meets these specifications is shown in Fig. 3.

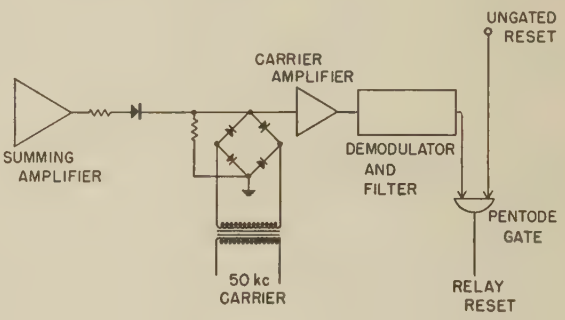

Fig. 3—Comparator circuit.

Basically the comparator which is shown in Fig. 3 consists of a wide-band, chopper-stabilized summing amplifier[7] which adds negative reference voltages to a positive input voltage. This amplifier has an over-all gain of 100 and a flat frequency response from dc voltage to 10 kc. Still further amplification of the sum of the input and the standard voltage is necessary before reliable operation of a gating tube may be obtained. To accomplish such reliability, a two-stage carrier type of amplifier is placed between the summing amplifier and the reset pulse gate. A bridge type of modulator[8] consisting of four germanium diodes modulates the 50-kc carrier which is then amplified and later demodulated. The output of the carrier amplifier is a dc voltage applied to the grid of a gate tube which passes reset pulses when a relay is to be reset. Within its linear region, the gain of this amplifier is approximately 50.

A germanium diode in series with the ring modulator passes only positive signals from the output of the summing amplifier. An increment of 1 millivolt at the input

[7] E. A. Goldberg, "Stabilization of wide-band direct-current amplifiers for zero and gain," *RCA Review*, vol. 11, p. 296; June, 1950.

[8] V. Belevitch, "Linear theory of bridge and ring modulator circuits," *Elec. Commun.*, vol. 25, p. 62; March, 1948.

to the summing amplifier corresponds to a change of 0.1 v at the output of the summing amplifier and to a change of approximately 5 v at the grid of the pentode gate.

The output of this comparator consists of a series of reset pulses which are generated as shown in Fig. 4 and which occur one-half of a digit period after relay closure. The top line shows the voltage at the grid of the gate tube, and the lower line, the resulting reset pulses. Corresponding binary-number output is shown on the last line.

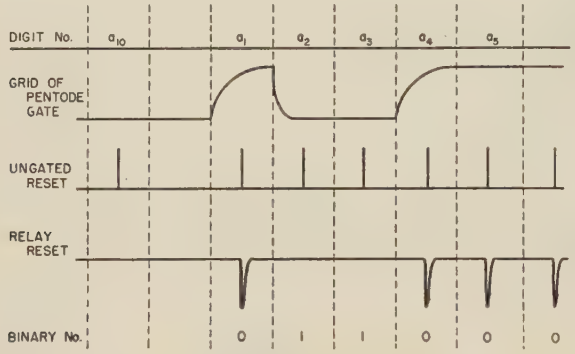

Fig. 4—Timing scheme for comparator gate.

B. Relay Selector Circuit

A ring circuit employing eleven thyratron stages supplies pulses necessary for relay operation and reset pulse gating, thus controlling the sequence of relay operations. Through a series of diode "and" gates, a reset pulse which is passed by the comparator gate influences only the relay which represents the digit under consideration. This reset pulse, when present, changes the state of a bistable multivibrator which in turn releases the relay. Relay current is supplied by a high-voltage supply with resistance in series so that essentially constant current is applied to the relay winding. Since the relay windings are highly inductive, the large initial voltage is desirable for rapid operation.

Fig. 5 shows the experimental two-channel encoder. Although systems of similar accuracy are available commercially, the sampling speed is too slow for use in rocket-motor instrumentation testing where tests are of short duration and a large number of points must be recorded. The encoder, together with the transcriber, provides a field recorder and an automatic-data-handling system capable of supplying engineering data of increased accuracy in a form which is easily handled by digital computing equipment.

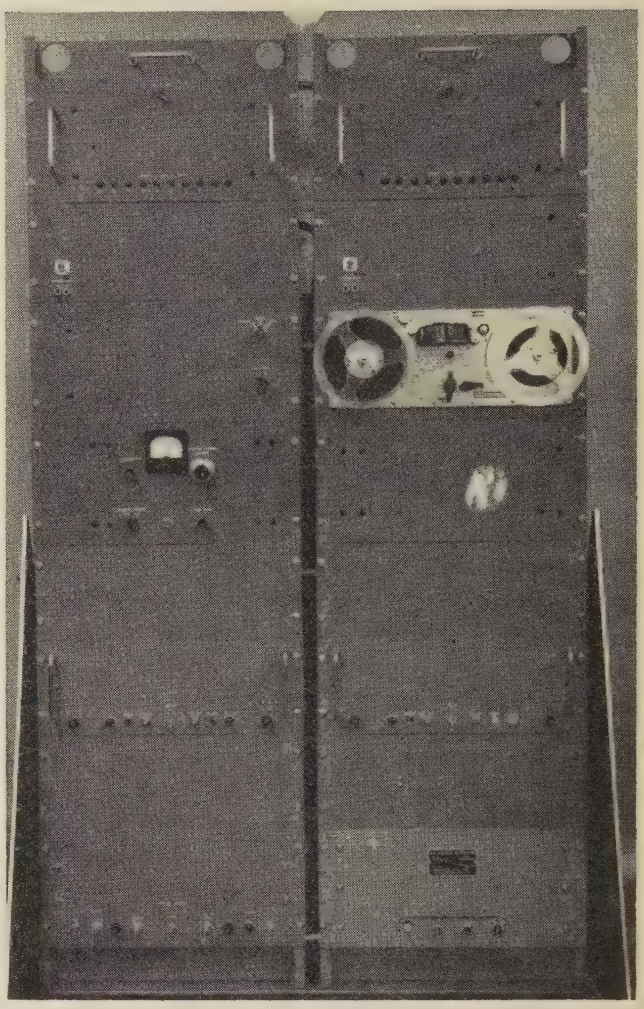

Fig. 5—Two-channel prototype encoder.

A New Method of Generating Functions

LAZARUS G. POLIMEROU*

Summary—**As a result of a pressing need for function generators, a new method of function generation has been developed. The underlying principle of this function generator is the application of ordinary pulse techniques in such a way as to produce a function. The simplicity of design, the high accuracy attainable, the simple type of construction are the outstanding features of this general-purpose function generator.**

In order to compare this new type of function generator with those presently being used, three important types are discussed. These generators are of the general-purpose, electric and photoelectric types; other comparable electromechanical types are excluded.[1]

Introduction

THE use of function generators in computational work is one of ever-increasing importance. The applications to the solution of complicated mathematical problems are numerous and varied.[2,3] The field of precise, high-speed electric and photoelectric type function generators is relatively new,[4–7] and is rapidly expanding with phenomenal results. Before considering the new-type function generator, a discussion is given on three other important types commonly in use today for the purpose of comparison.

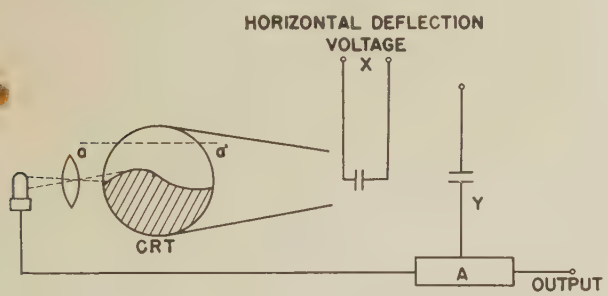

Fig. 1—Electrostatic deflection type photoformer.

One of the earliest of these types of function generators is shown in block diagram form in Fig. 1. The dependent function mask is placed in close juxtaposition to the plane of the phosphor; or the plane of the phosphor is projected by a suitable optical system into the plane of the mask.

A bias voltage is used to position the spot along the line a-a' in Fig. 1. This line is everywhere above the edge of the mask and is the reference line of the function displayed on the mask. A feedback loop is phased so that increasing light on the photo-tube causes the spot to move downward. Given suitable optical shielding and sufficient over-all gain, the spot will be constrained to adopt a position whereby a substantial fraction of light from the spot is obscured by the mask.

When the spot is in the plane of the mask as described above, small changes of spot height away from the equilibrium position tend to cause large changes of light on the photo-tube. The spot, therefore, will reach equilibrium very nearly at the height of the mask.

If the deflection sensitivity of the cathode-ray tube (CRT) is independent of beam height, which is ordinarily the case, the output voltage is proportional to the spot height. The time necessary to reach equilibrium around the feedback loop is determined by the total delay time around the loop. This delay time includes the decay time of the phosphor plus the delay time of the amplifier and the photo-tube.

It will be noted that the persistence of the screen, the afterglow, corresponds to an integrating term in the feedback loop, setting an upper limit both to the frequency response and to the gain of the amplifiers in accordance with the Nyquist criterion of stability.[8]

If $y = F(x)$ be the equation of the mask relative to the deflection axis, and if the spot is deflected linearly with time in the X-direction, the output waveform will be an electrical replica of the edge of the mask. To be more specific, if the co-ordinates of the mask are (x, y) and the voltages on the Y_1, Y_2, X_1, X_2 plates are p, q, r, and s respectively, we have

$$p - q = \frac{y}{k_1}; \qquad r - s = \frac{x}{k_2}$$

where k_1 and k_2 are normally constant, being inversely proportional to the accelerating voltage, V, of the tube. Hence the output voltage p will obey the law

$$p = q + \frac{1}{k_1} \cdot m[k_2(r - s)] \quad \text{with} \quad m \propto \frac{y}{x},$$

where q, r, and s (and to a limited extent k_1 and k_2) are independent variables and m includes the rotation and displacement of the axes with respect to which the curve was originally drawn.

The main features of this type function generator are:[6]

(1) A 10-microsecond-per-inch rise time corresponding to a 150-kilocycle-per-second high-frequency cut-off.

* Ordnance Electro-Mechanical Laboratory Division, White Sands Proving Ground, N. M.

[1] P. R. Vance and D. L. Hass, "An input-output unit for analog computers," PROC. I.R.E., vol. 41, pp. 1483–1486; October, 1953.

[2] H. W. Schultz, "The photoformer in anacom calculations," *Proc. NEC*, vol. 5, p. 40–47; 1949.

[3] E. J. Hancock, "Photoformer design and performance," *Proc. NEC*, vol. 7, pp. 228–234; 1951.

[4] D. M. Mackay, "A high speed electronic function generator," *Nature*, vol. 159, p. 406; March, 1947.

[5] D. J. Mynall, "Electronic function generator," *Nature*, vol. 159, p. 743; May, 1947.

[6] D. E. Sunstein, "Photoelectric waveform generators," *Electronics*, vol. 22, pp. 100–103; February, 1949.

[7] A. B. MacNee, "An electronic differential analyzer," PROC. I.R.E., vol. 37, pp. 1315–1324; November, 1949.

[8] H. Nyquist, "Regeneration theory," *Bell Sys. Tech. Jour.*, pp. 126–147; January, 1932.

(2) The degree of accuracy is given for the static case for a feedback loop with a gain of the order of 40 db or greater. The position of the spot will generally coincide with the mask displacement to an accuracy of better than ± 1 per cent.

(3) Also, double-valued functions can easily be used, whereby increasing and decreasing voltages permit switching paths on the function, Fig. 2.

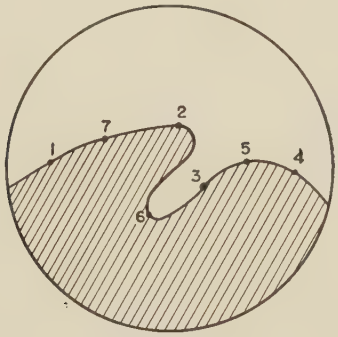

Fig. 2—Function mask.

A second type of function generator using a magnetic type deflection is found in Fig. 3. The screen of a CRT (Flying Spot Scanner)[9] is optically projected on a graph specimen. A bias voltage is supplied to the vertical deflection circuits of the CRT which voltage by itself is sufficient to drive the spot to the bottom of the tube.

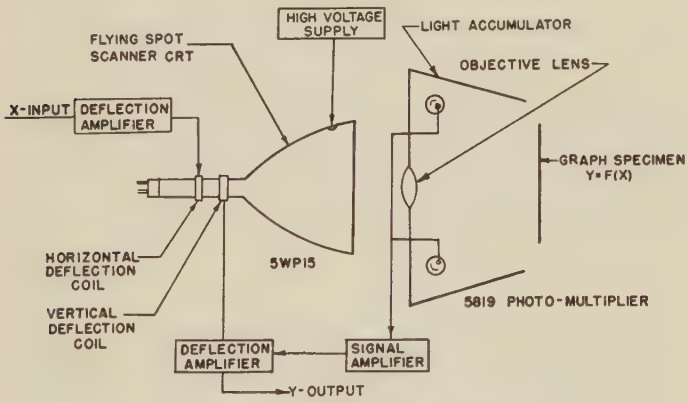

Fig. 3—Magnetic deflection type photoformer.

However, light reflected from the white portions of the graph (Fig. 4), is picked up by a bank of photo-multiplier tubes, and the voltage generated by the photo-multiplier tubes is fed back to the deflection amplifier so as to drive the spot to the top of the CRT. If there exists a sharp line of demarcation between white and dark portions of the graph sheet, the spot of light will reach an equilibrium position where the line of demarcation will divide the spot permitting just sufficient light to reflect from the white portions of the graph to maintain equilibrium. In this way, the spot of light is made to follow a white line on a dark-background graph sheet. An independent voltage controls the horizontal or X-position on the graph sheet and the vertical or Y-position output voltage is obtained at a convenient position in the vertical deflection amplifier circuit.

The main features of this type of function generator[10] are high accuracy, rapid response (amplitude and phase characteristics are essentially flat beyond 100 cycles per second), and ease of function-specimen preparation.

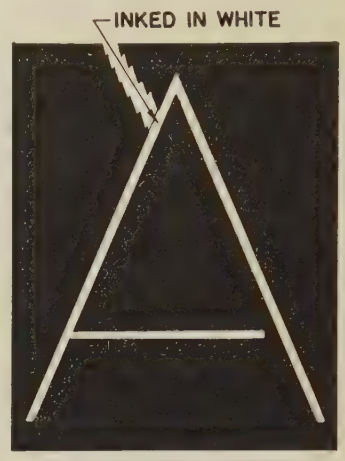

Fig. 4—Double-valued function.

Both the function generators heretofore mentioned have several limitations in the arbitrary forcing of a dependent variable. Among these limitations are:

(1) The finite spot size results in some distortion for which compensation is difficult; since distortion depends on the gain of the amplifier, the intensity of the spot, the height of the pattern, the location of the quiescent position, etc., all of which vary from time to time;

(2) Halo effect of screen—which may cause clipping of high peaks of the template; and

(3) Parallax.

Careful proportioning of over-all height and width of the pattern, location of the quiescent position, and adjustment of gain minimize these difficulties but definite limitations of accuracy exist.

Another type of function generator[11] is one that approximates the function by a series of small segments. This type (shown in Fig. 5) is not truly a general-purpose function generator, but it can handle many useful functions. A restriction is imposed in this type of function generator in that the value of the function must always change in a unilateral direction, as the input varies.

Referring to Fig. 5, the variable resistors are made to have a relatively large value compared to the forward

[9] "Flying spot video generator," ed. Vin Zeluff, *Electronics*, vol. 21, pp. 124–126; June, 1948.

[10] C. N. Pederson, A. A. Gerlach, and R. E. Zenner, "A precise electronic function generator," *Proc. NEC*, vol. 7; 1951.

[11] G. D. McCann, C. H. Wilts, and B. N. Locanthi, "Electronics techniques applied to analog methods of computation," Proc. I.R.E., vol. 37, pp. 954–961; August, 1949.

impedance of the crystals, so that variations of crystal impedance with changes in current cause a negligible change in the over-all impedance. Functions may be generated in three ways by means of this circuit.

The first method considered produces a curve of decreasing positive slope. If all the switches are thrown to the left, each parallel branch will conduct current when the terminal voltage rises above the battery voltage of that branch. By setting the proper value of battery voltage in each branch, certain switch-points are chosen which best fit the desired function. A current-voltage characteristic shows a series of straight lines with the slope of successive segments decreasing as the voltage rises, as shown by Curve 1 of Fig. 6.

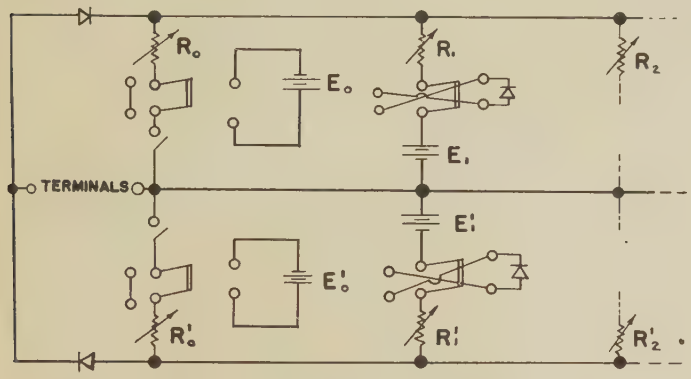

Fig. 5—Segment function generator.

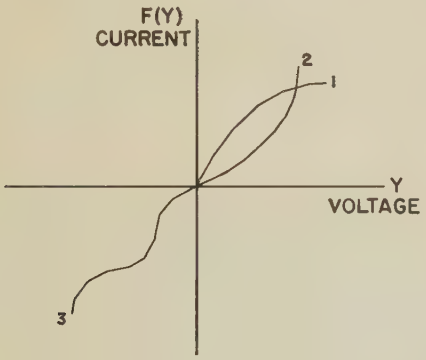

Fig. 6—Segment function generator characteristics.

The second method produces a curve of increasing positive slope. When all the switches are thrown to the right, each branch produces a circulating current which passes through R_0. The battery voltage, E_0, is provided to give zero terminal voltage when no external current enters the terminals. As voltage is applied, the current which flows is determined by the effective resistance of all branches in parallel. As the terminal voltage rises above the branch battery voltage, the current in the branch ceases to flow, and the effective impedance of the device is increased. When the voltage is sufficiently high to cause current flow to cease in the branches, the impedance of the device is equal to R_0 alone. The current-voltage characteristic is one of constantly increasing slope, as shown by Curve 2 of Fig. 6.

Combinations of alternately increasing and decreasing portions of curves can be made, provided that the slope always remains positive. (See Curve 3 of Fig. 6.) A generator of this type can fit curves using 22 parallel branches; 11 for positive voltages and 11 for negative voltages with good accuracy. Of course the main disadvantage of this method is that it is limited to only certain types of functions.

The next function generator to be discussed is the main topic of this paper and constitutes a new approach to the problem of generating functions. This approach utilizes an open-loop method of operation that has considerable merit.

Principle of Operation

The basic function generator is composed as follows: An electron beam of a CRT is made to scan a mask (as shown in Fig. 7) at a relatively high sweep rate; approximately 2000 cps is used in the present model. As the beam passes the reference line of the mask, a pulse is produced by a photo-multiplier tube, which looks only at this reference line. The beam continues to move and scans past the function line of the mask, whereupon a second pulse from a second photo-multiplier tube, looking only at the function line, is produced. The time delay between these two pulses is directly proportional to the length of the ordinate between the reference line and the function line, assuming a linear sweep. These two pulses are then shaped and fed into grids of a flip-flop circuit (Binary Scalar 102) which produces a square wave that has a width proportional to the time delay between the pulses and that has a constant amplitude. In this process, the first pulse initiates the square wave and the second pulse terminates the square wave. Thus a train of square waves is produced. The square waves have a fundamental frequency of approximately 2000 cps. The square waves are then rectified and integrated, thus producing a varying dc voltage that is proportional to the ordinate between the reference line and the function line; i.e., a voltage proportional to the value of the function at the point being scanned.

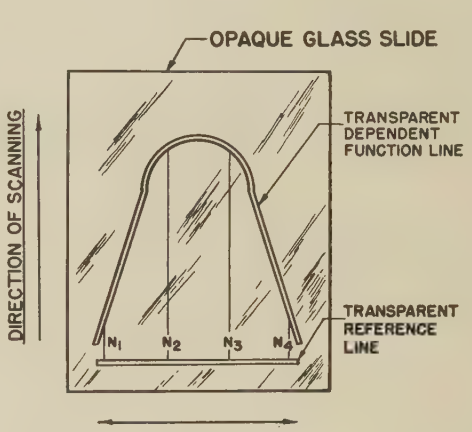

Fig. 7—Independent voltages ($N_{1,2,3,4}$ are several ordinates).

As the ordinate length varies, so does the output voltage. By moving the scanning line (in a direction perpendicular to the scan, called the independent function axis) over the mask, which represents the dependent function, the ordinate lengths can be made to vary with respect to the position of the scan. If the scanning line is moved in a linear fashion with respect to time along the independent axis, a voltage is produced in the output, which is the electrical replica of the mask, as given in Fig. 7. Furthermore, the scanning line can be moved in a nonlinear manner, along the independent function axis, thus producing a function of a function.

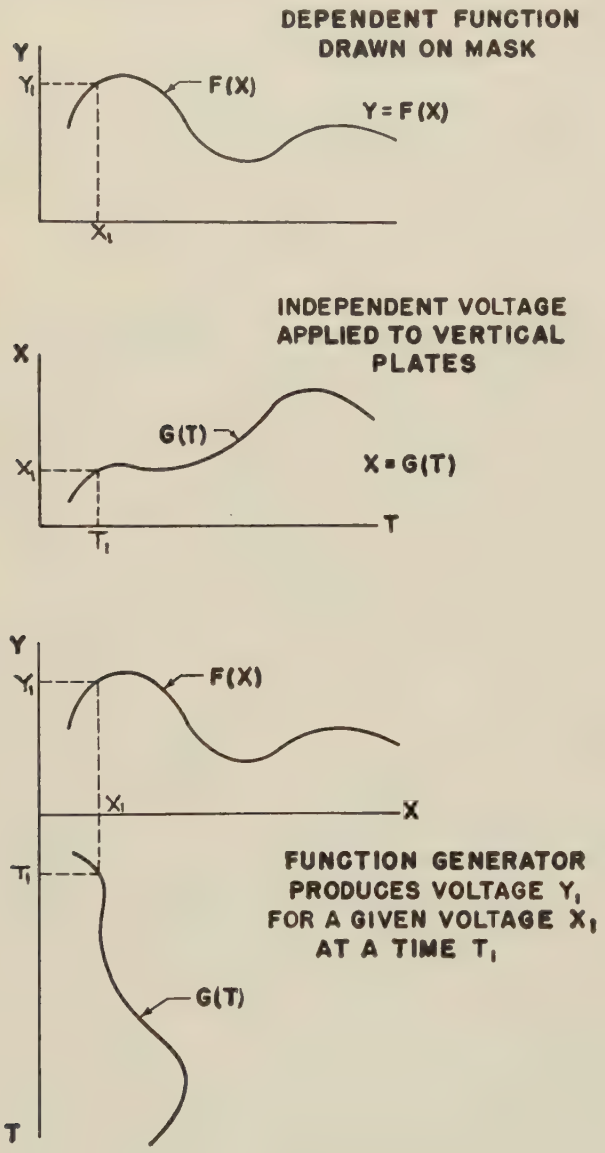

Fig. 8—Graphic analogy.

A graphic representation of what the function generator does is given in Fig. 8. At a particular time value, there is a corresponding value of the X-variable, for which, in turn, there is a corresponding value of Y-variable. Thus, $Y = F(X)$ when $X = G(t)$. The function generator automatically produces a voltage, Y, for a voltage, X, at the time, t.

Technical Details

A consideration of the type of phosphor screen of the CRT led to the use of the 5LP5 tube. This tube displays a very short persistence characteristic in the blue-violet portion of the spectrum. The 931A photo-multiplier tube was used because of its high gain as well as for its sensitivity to the same blue-violet portion of the spectrum. No optical system was used. The dependent function with its reference line was drawn on paper such that its maximum dimension was no longer than $2\frac{3}{4}$ inches. A photograph was then prepared for a standard $3\frac{1}{4} \times 4$ inch glass slide which was entirely opaque except for transparent reference and function lines. The function generator consists of four individual function generators.

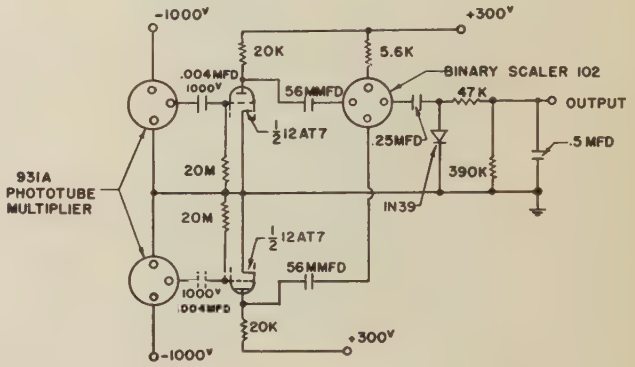

Fig. 9—Function generator.

Electric Circuitry

The main part of the function-forming device is quite simple (Fig. 9). It provides for the use of two 931A photo-multiplier tubes, which are operated by −1000 volt supply. A common sweep and synchronizing circuit is used. Voltage to operate the 12AT7 is provided from

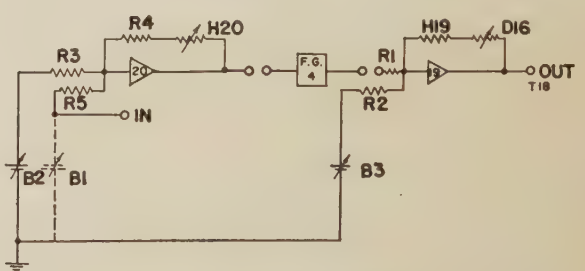

Fig. 10—Scale factor adjustment.

an external source. The 12AT7 is used to clip the large voltage pulse from the photo-multiplier tube, producing an amplified clipped pulse that is free from variations of light intensities. The pulses are sharpened by passing through a small-valued capacitor and are fed into a flip-flop circuit. The value of these sharpened pulse-voltages is just at the minimum level for tripping the flip-flop. The rectifier is used to establish a voltage reference for the signal after it has passed through the dc isolating capacitor from the flip-flop. An integrating circuit is then used to produce a voltage proportional to the varying widths of the square wave. External scale-factor adjustment circuits are used (Fig. 10).

In addition to this model design, it is recognized that by employing amplitude modulation at the output of the flip-flop circuit, a function of a function, multiplied simultaneously by another function can be obtained. More combinations also exist.

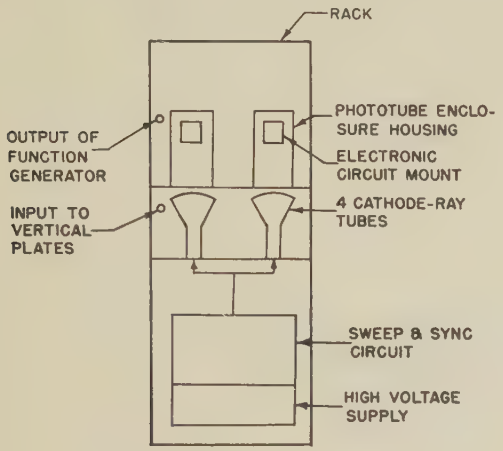

Fig. 11—System arrangement.

Mechanical Design

Four function generators are mounted vertically in a standard-size metal cabinet. The cathode-ray tubes are mounted on one metal sheet and the photo-multiplier tube housings on another metal sheet, such that the end of the CRT touches the glass slides which are inserted at the base of the photo-multiplier tube housing. (See Figs. 11 and 12.) The ends of the housings are removable for visual inspection of the initial positioning of the scan. (High voltage is shut off for this operation.) The function-generating circuits are built onto the housings. The input and output jacks are located in the back of the cabinet, and the glass slides of the functions are also inserted from the rear. (See Fig. 12.)

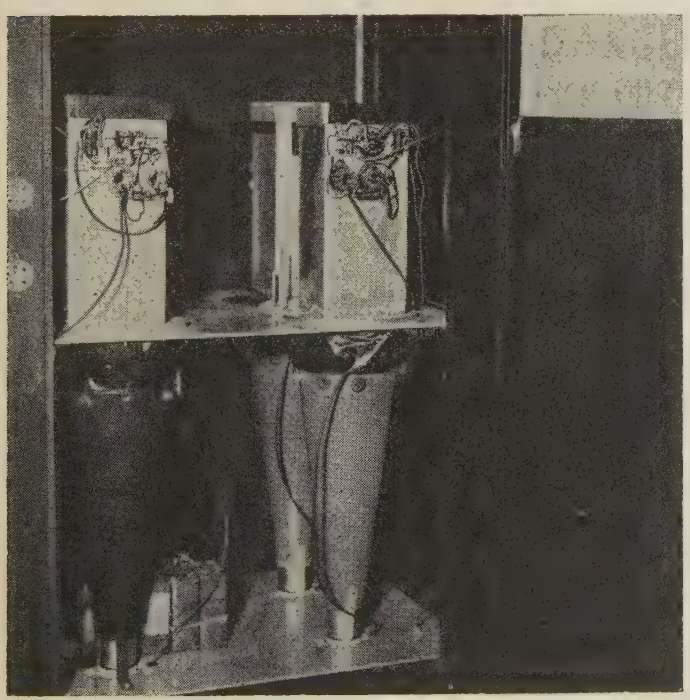

Fig. 12—Rear of function generator cabinet.

Features of the System

In the existing model of the new function generator described, an accuracy of ± 1.5 per cent was obtained. The frequency response obtained was flat up to 7 cps for the independent variable. See Fig. 13, which shows one of the several units mounted in cabinet. The method of function specimen preparation is highly effective. No optical system is used. The design lends itself to easy fabrication techniques and is therefore economical.

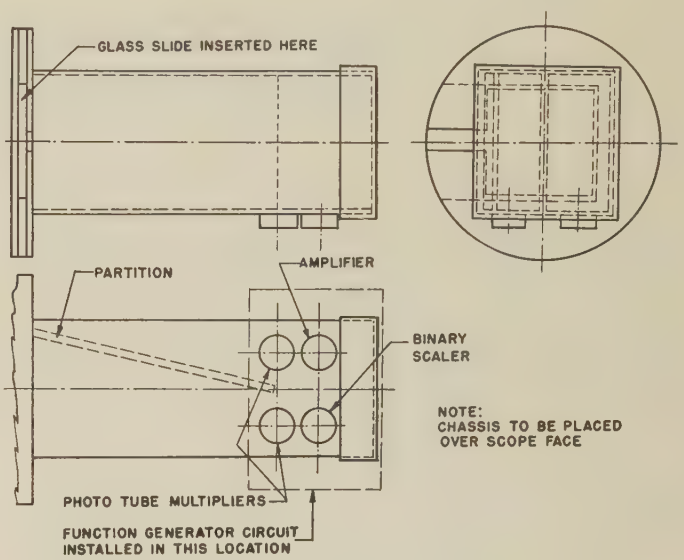

Fig. 13—Photo tube chassis.

The principal design limitation is the result of the inherent time delay introduced in scanning the function. A high frequency response must account for the time necessary to scan the function plus the time delay of the integrating circuit. This means that a very high scanning frequency must be used to reduce the time for scanning the function. Other present design limitations can be altered somewhat by a consideration of the errors that are involved.

An analysis of the error in the function generator shows that a major part of such error can be attributed to parallax due to the curvature in the face of the CRT used in this model. As a result, it is evident that a major portion of the error can be eliminated by merely switching to a flat-faced CRT. Or preliminary steps can be made to take this sort of error into consideration when drawing up the functions, thereby cancelling the effect of error. Still greater accuracies can be attained by the use of precision cathode-ray tubes. Further correction can be made by the use of finer and more accurate pulse forming circuits, at the expense, however, of simplicity of construction.

Conclusion

It is believed that with proper design considerations a function generator of this type can be built with an accuracy of better than ± 0.5 per cent and a flat frequency response greater than 100 cps. The present model was designed for use in the solution of free-flight rocket trajectory problems using a slowly changing independent voltage-variable and having an accuracy between 1 and 5 per cent. This model was completed in January, 1953, and is currently being used by the Computer Section, Electro-Mechanical Laboratories Division, at White Sands Proving Ground, Las Cruces, New Mexico, in the solution of analog computer problems. A patent on this experimental model is being sought.

Acknowledgment

Appreciation is expressed to Richard Clay, Michael Keenan, and Joseph Christ for their suggestions.

A Function Generator for the Solution of Engineering Design Problems

C. J. SAVANT* and R. C. HOWARD†

Summary—**The solution of nonlinear engineering design problems demonstrates the need for a special function generator. The generator described in this paper satisfies this need. The basic components of the unit are discussed and the forms of functions which can be generated are shown. Accuracy is estimated by comparison of an oscillogram with the calculated curves. It is concluded from tests on the system that the function generator is a valuable aid in the handling of nonlinear design problems.**

Introduction

THE ENGINEER need not look far in his work to find a nonlinear problem. The mechanical engineer knows that springs and dashpots are linear in only small regions. Familiar stress-strain diagrams, gas-expansion laws, and even the simple pendulum cannot be described in all regions by linear equations. The electrical engineer is familiar with the saturation of iron-core inductors, nonlinear vacuum-tube characteristics, and curved torque-speed curves of servo motors. These are just a few of the common relationships which engineers usually linearize in order to obtain a solution based on classical linear theory. Practically all of the characteristics of nature are nonlinear, and the linearizations commonly practiced are approximations, valid only in restricted regions.

Mathematicians have attacked the second-order nonlinear differential equation, and some results have been obtained with iteration and perturbation techniques.[1] The problem becomes unwieldy even for small nonlinearities, and hence these methods are not satisfactory for use by engineers. Since the convergence of these methods often depends upon the nonlinearity being small, the methods are not even applicable when the nonlinearity is large. Numerical integration can always be performed, but the labor involved in finding just one solution is often prohibitive. Topological methods[2] have aided in the solution of second-order systems, but little has been done with higher-order equations by graphical techniques.

Both analog and digital computers have been employed by engineers in the solution of nonlinear equations. In many of these solutions, considerable time is expended in setting the nonlinearity into the computer. Existing techniques do not lend themselves to easy change of the nonlinear function.

The need for a versatile arbitrary function generator of a dependent variable is strongly felt in feedback control system design. For example, consider a control system, the response of which requires improvement. It may be possible to better the performance if appropriate nonlinear functions be added, either in the forward loop or in the feedback path. In determining the nature of this nonlinear function, one is not so concerned with a high degree of accuracy as in the ease of modifying one function into another in an attempt to discover an optimum. The nature of the design problem demands a highly versatile function generator with only a reasonable accuracy (perhaps 5 per cent) required.

The arbitrary function generator discussed in this paper satisfies the needs of the designer in that the form of the permissible nonlinearities can be changed by the setting of two knobs.

The present function generator boasts another advantage. In many problems it may be necessary to generate products of arbitrary functions of two or more variables. The unit described in this paper permits products of the general form

$$[f(x)]^{\alpha}[g(y)]^{\beta}[h(z)]^{\gamma}$$

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† Bell Telephone Labs., 463 West St., New York, N. Y.

[1] J. J. Stoker, "Nonlinear Vibrations in Mechanical and Electrical Systems," Interscience Publishers, Inc., New York, N. Y.; 1950.

[2] N. Minorsky, "Introduction to Nonlinear Mechanics," J. W. Edwards Brothers, Inc., Ann Arbor, Mich.; 1947.

where $f(x)$, $g(y)$, and $h(z)$ may be the dependent variables of a given problem or may be any independent variables. The exponents α, β, and γ may be either positive or negative.

Principles of Operation

The principle of operation of the generator is based on the logarithmic function, which has the following property:

$$\alpha \log_a f(x) + \beta \log_a g(y) + \gamma \log_a h(z) = \log_a \{[f(x)]^\alpha [g(y)]^\beta [h(z)]^\gamma\} \quad (1)$$

where "a" is a real positive number.

Since summation is an easy operation with electronic circuits, the logarithms of three voltages can be added simply, and the taking of the inverse logarithm of the sum results in the product. Hence the difficult operation of analog multiplication (or division) is performed easily by adding voltages. Thus the first and most important work centered about the development of two electronic circuits which have the required logarithmic and inverse logarithmic characteristics. This development resulted in two basic units: the log-taking element (LTE), the output of which is the negative logarithm of the input voltage, and the inverse-log-taking element (ILTE), the output voltage of which is the inverse logarithm of the input. These two units plus necessary polarity inverting equipment comprise the arbitrary function generator of a dependent variable (subsequently called AFDEV).

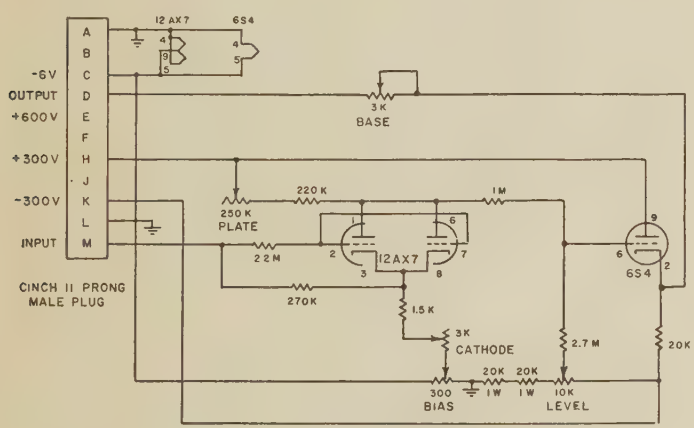


Fig. 1—Circuit diagram of LTE.

Linear-to-Logarithmic Converter

The log-taking element (LTE) is an electronic converter whose output is the negative logarithm of the input voltage. The circuit diagram of this unit is given in Fig. 1. The details of the LTE have been reported in a previous paper.[3] The important facts to know in connection with the LTE are that for positive input voltages from 0.3 to 300 volts the output has the form:

$$-\log_a e_{in}.$$

[3] R. C. Howard, C. J. Savant, and R. S. Neiswander, "A linear-to-logarithmic converter," *Electronics*, vol. 26, p. 156; July, 1953.

The output voltage varies over a range of +3.0 to −30 volts with a logarithm base, a, of approximately 1.20.

The LTE units are interchangeable and a drift stability of 75 mv/hr at the output is attained by 500-hour tube aging. The accuracy of the logarithmic function can be verified by reference to Fig. 2 where the static characteristic is plotted on semi-logarithmic paper.

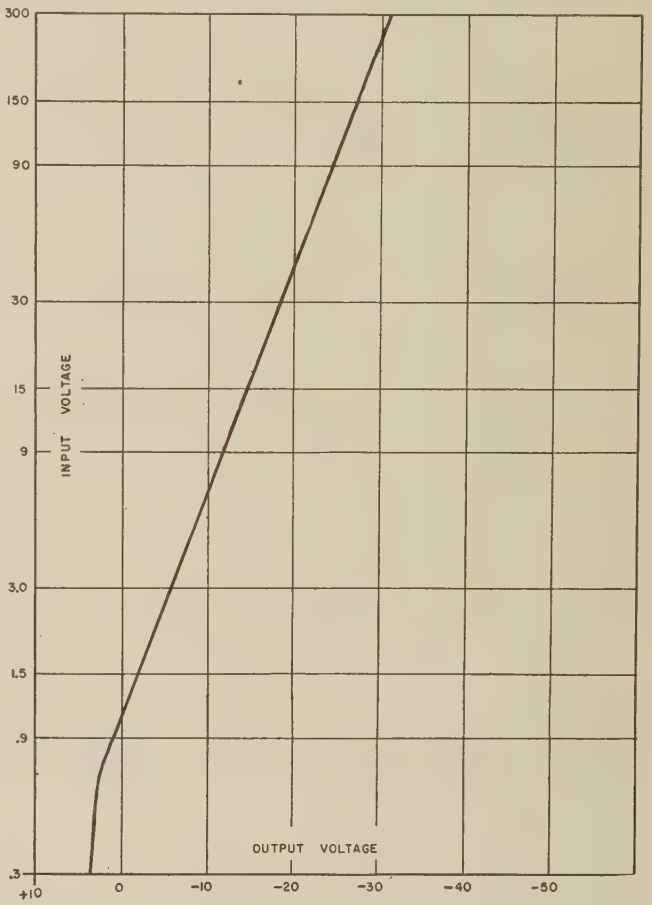


Fig. 2—LTE characteristic plotted on semi-log paper.

Inverse-Log-Taking Element

The underlying concept governing the operation of the inverse-log-taking element, hereafter known as the ILTE, is simple, namely, use of a high-gain amplifier with an LTE in the feedback loop. The operation can

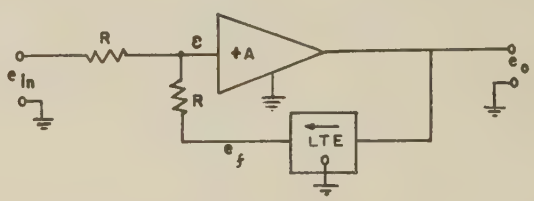


Fig. 3—ILTE block diagram.

best be understood from a consideration of Fig. 3. With the symbols defined on the figure, one can readily write the following basic equations of the circuit:

$$\epsilon = \frac{e_f + e_{in}}{2} \quad (2)$$

$$\epsilon A = e_0 \tag{3}$$

$$-\log_a e_0 = e_f \quad \text{(valid if } e_{in} > 0\text{)}. \tag{4}$$

Combination of (2), (3), and (4), results in the expression:

$$\epsilon = \tfrac{1}{2}[-\log_a e_0 + e_{in}] = \frac{e_0}{A}. \tag{5}$$

If A is very large, and positive, (5) reduces to

$$e_0 = \exp_a e_{in}. \tag{6}$$

Eq. (6) demonstrates that the output voltage of the ILTE is proportional to the inverse logarithm of the input voltage.

A more complete analysis shows that

$$e_0 = \exp_a\left[\{e_{in}\}\{1+(\Delta+2\delta)\ \ln\ a\}\left\{1+\frac{2}{A}e_0 \ln a\right\}\right] \tag{7}$$

where

δ = drift voltage of amplifier referred to the input.

Δ = drift voltage of LTE referred to the output and A is large but not infinite.

From (7) approximate per cent-error expressions resulting from drift and insufficient gain can be obtained as follows:

$$\text{Per cent error from drift} = E_d \doteq 100(\Delta+2\delta)\ \ln\ a. \tag{8}$$

$$\text{Per cent error from lack of gain} = E_g \doteq 200/A e_0 \ln a. \tag{9}$$

With nominal values ($\Delta = 50$ mv, $\delta = 25$ mv, $a = 1.20$, $e_0 = 300$ v, $A = 8000$) substituted in (8) and (9), the maximum possible errors are

$$E_d = 2.3 \text{ per cent} \qquad E_g = 2.1 \text{ per cent}. \tag{10}$$

One should realize, however, that with appropriate adjustment of the final unit, E_d can be reduced considerably, and E_g can be eliminated completely. Switches and terminals which are located on the front panel make the LTE input and output terminals readily accessible. If the LTE is adjusted in the normal manner, only minor changes are necessary when the loop is closed. With static input voltages applied, the response (Fig. 4) can be determined accurately. The log base of this response curve is computed from the straight line to be 1.20. The drift of the ILTE has been observed in operation to be about 1 volt per hour with 3.0 volts out and 3 volts per hour with 300 volts out.

Polarity Inverting Problem: Input

From a purely mathematical point of view, the logarithm of a negative number is complex. When presented with negative input signals, the electronic LTE, however, produces incorrect output voltages since the LTE functions much the same as an amplifier when the grid signal is negative. The response of the LTE is proportional to the logarithm of the input voltage for positive

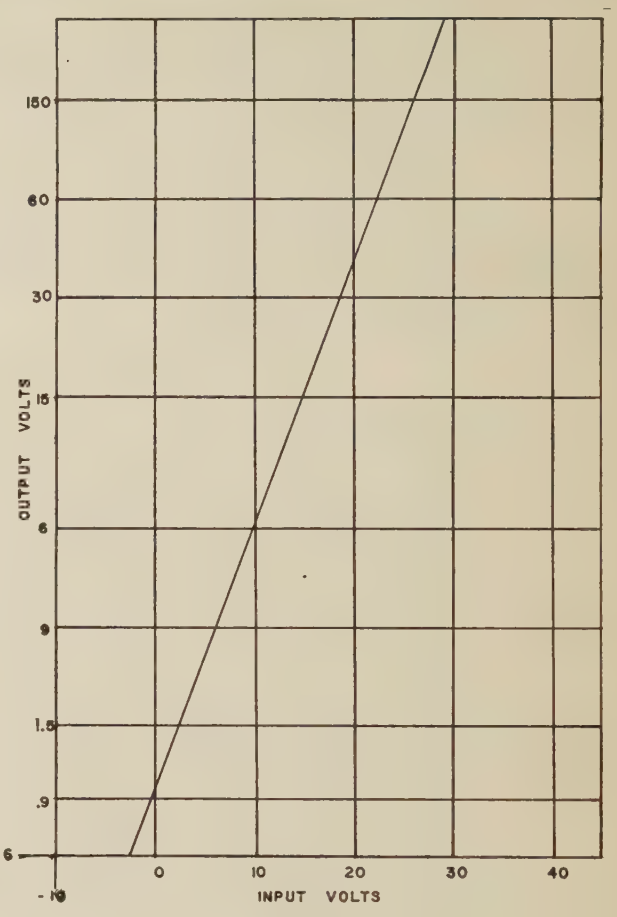


Fig. 4—Response of ILTE.

applied voltages from +0.3 volt to +300 volts. For values less than 0.3 volt, the response is no longer logarithmic. To avoid the negative-signal difficulty, the system shown in the block diagram of Fig. 5 was developed. The signs of all input signals are converted to a positive sense and in this form are sent through the

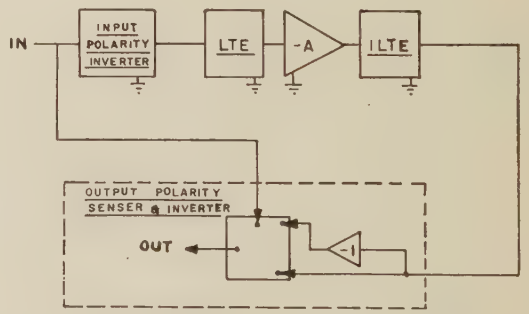


Fig. 5—Block diagram of system.

LTE and the remainder of the computer. At the output of the computer, the all-positive signals and the all-negative signals which are obtained at the output of a negative gain amplifier are sent into the output polarity inverter. A polarity senser is used to measure the sign of the input and to switch electronically the positive or negative signal to the output, depending on the input polarities. The appropriate sign of the resulting output has thus been restored.

The input inverter unit operates much the same as a full-wave rectifier. For varying input voltages in the range −150 to +150 volts, the output voltage is positive. The gain is approximately 0.7, with a gain stability $\Delta A \leqq \frac{1}{2}$ per cent. The drift voltage of the output is less than 0.3 volt.

Polarity Inverting Problem: Output

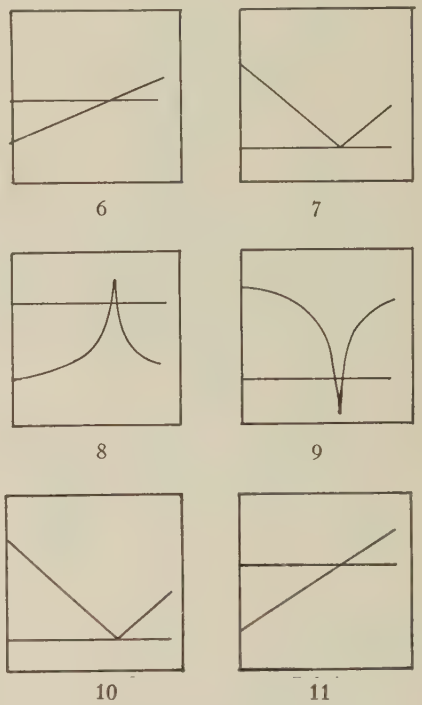
The output polarity inverter includes all equipment enclosed in dashed lines on Fig. 5 and, because of its logical system, is more complicated than the input inverter. The heart of the inverter is a pair of amplifiers; one inverts the input signal, and the other does not. The sensing part of the inverter allows only one amplifier to operate at a time, thus controlling the polarity of the output. Input signals applied to the sensing input terminals control the sensing circuit in such a manner that the correct algebraic sign is restored to the output. Consider, for example, the multiplication of two voltages. If both input voltages have the same polarity (i.e., both negative or both positive), then the output voltage should be positive. If, however, the two input signals have opposite signs, then the output voltage should be negative.

Since the ILTE, like the LTE, operates only on positive signals, the input to the output polarity inverter is always positive. In testing, one always applies a positive voltage because the device will give meaningless outputs for negative inputs. The sensing input terminals of the inverter are connected at points in the circuit where the signals to be multiplied have proper signs (i.e., before the input polarity inverter), and the correct signs of the signals passing through the output inverter are again restored.

Two switches, labeled input bias, are mounted on the front and permit the use of the inverter with only one applied signal. When only one voltage is to be inverted, a constant voltage is applied to the other sensing channel with the input bias switch.

Complete System

Fig. 5 presents a typical connection of the four basic elements in a complete system. To demonstrate the shape of the function at the intermediate points of the arbitrary function generator, Figs. 6 to 11 were prepared. Fig. 6 demonstrates the input to the AFDEV which is obtained from a linear-sweep generator. The oscillogram of Fig. 7 presents the output voltage from the input polarity inverter. Notice that in this and all other photographs of this group, the zero trace was established by means of a double exposure. Figs. 8 and 9 show the output of the LTE and the negative-gain amplifier, respectively. The gain of the amplifier was set to unity so that a direct comparison, input vs output is possible. Fig. 10 shows the output of the ILTE, and Fig. 11 presents the output of the polarity inverter and hence the output of the AFDEV. In this last demonstration an exponent of 1 was established. Use of a gain other than unity, together with an attenuating potentiometer, provides the possibility of a range of exponent ($\frac{1}{5}$ to 5). In the next section this system is used to generate arbitrary functions of an independent variable.



Figs. 6–11—Figures demonstrating waveforms at various points through the system.

Arbitrary Function of an Independent Variable

Although the nonlinear computer finds its primary use as an arbitrary function generator of a dependent variable (AFDEV), the multiplier also can act as an arbitrary function generator of an independent variable

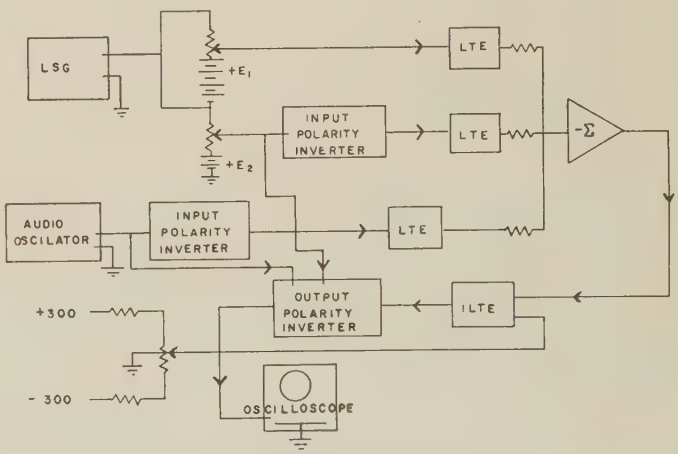


Fig. 12—Block diagram of AFINV.

(AFINV). In this latter application, the nonlinear computer competes both in accuracy and in versatility with the existing arbitrary function generators. To demonstrate a few of the driving functions obtainable with the AFINV, the system shown in the block diagram of Fig. 12 was set up. With this arrangement the

outputs of three log-taking elements are summed and fed to the LTE. A linear sweep added to a constant voltage E_1 and E_2 drives two LTE's with functions of the form.

$$y_1 = A(x + a) \quad \text{and} \quad y_2 = B(x + b). \tag{11}$$

The third LTE is driven with an audio oscillator which provides a function

$$y = c \sin kx. \tag{12}$$

To prevent the LTE signal from becoming negative, the input polarity inverters are appropriately inserted. Only two inverters are necessary since one signal is always positive. An output polarity inverter is used to restore the correct sign to the output signal which is displayed on an oscilloscope.

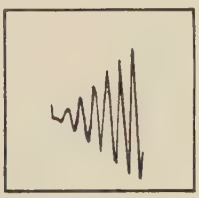


Fig. 13—$x \sin kx$.

Fig. 14—$x^n \sin kx$ $(n<1)$.

Fig. 15—$x^n (\sin kx)^m$ $(n>1, m \ll 1)$.

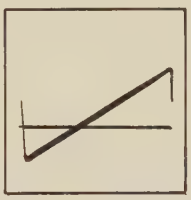


Fig. 16—$(x-a)$ input to system.

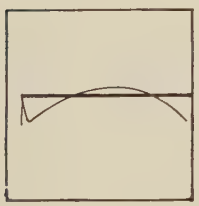


Fig. 17—$(x-a)^n (x-b)^m$.

Fig. 18—$x(x-a)(x-b)$.

As connected, the function generator provides functions of the form

$$y = A(x + a)^{\alpha}(x + b)^{\beta}(\sin kx)^{\gamma}. \tag{13}$$

If other functions $g(x)$, $h(y)$, and $f(z)$, are supplied to the LTE units, the more general function

$$y = A[g(x)]^{\alpha}[h(y)]^{\beta}[f(z)]^{\gamma} \tag{14}$$

is possible. Various functions of the form (13) are demonstrated in the AFINV oscillograms of Figs. 13 to 18.

A cursory glance at the available possibilities shows the versatility of the nonlinear function generator.

In an effort to ascertain the accuracy of the generator the function $y = Ax^n$ ($A = 3$ and $n = 0.5$) was set up on the computer. This step was accomplished by removing all but one LTE in Fig. 12. From an enlarged copy of the oscillogram shown on Fig. 19 the points were plotted on log-log paper (Fig. 20). From the resulting straight line, the curve was determined to be

$$y = 2.98x^{0.488}.$$

Comparison of the exponent yields a discrepancy of 2.4 per cent between the two expressions, with the constant multiplier in error by 0.7 per cent. From the scatter of the points the error is estimated to be 3 per cent. Since judgment is required in reading the oscillogram, this last value might be improved with practice.

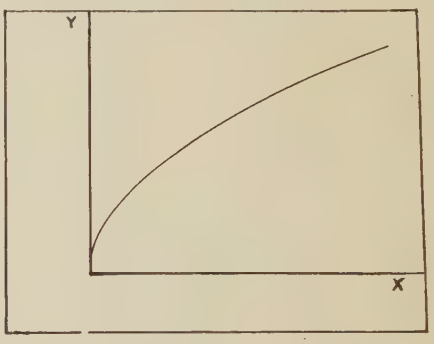


Fig. 19—Enlarged view of oscillogram.

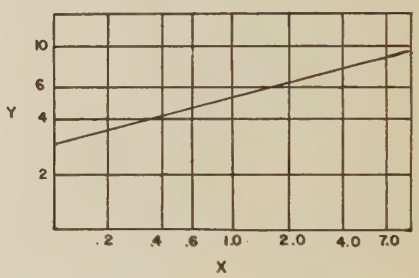


Fig. 20—Log-log plot of Fig. 19.

Conclusions

The unit described is capable of producing a large variety of nonlinear functions. It is especially important to notice that any functional voltage in an analog computer can be used as the input to the function generator and hence can be multiplied by any other function, raised to a desired power. This advantage provides a useful tool in engineering analysis. A subsequent paper will outline the solutions of nonlinear control system problems wherein this function generator was used.

news

New Chapters

Dallas-Fort Worth and Akron have been added to the growing list of chapters included in the last issue of the Transactions. There is now a total of 11 active chapters of the PGEC throughout the country. If there is no chapter in your area and there is sufficient interest in computers to warrant establishing one, please write to the editor of this column.

PGEC National Officers and Committee Chairmen, 1954–55

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Joint Computer Conference

The 1954 "Eastern Joint Computer Conference and Exhibition" will be held on December 8, 9 and 10 at the Bellevue Stratford Hotel, Philadelphia, Penna. The theme of the conference this year will be "The Design and Application of Small Digital Computers." Advance registration for members of the participating societies will be $3.00, which includes a copy of the proceedings. Tours of the many computer laboratories in the Philadelphia area, several of which have increased their facilities since the 1951 Philadelphia Conference, will again be provided.

Membership

With an ever increasing total paid membership (to date over 2,500), the PGEC is now the largest Professional Group of the I.R.E. The membership committee has prepared a brochure containing some good reasons for joining the PGEC and an application blank. Copies are available in quantity from Mrs. Gene Duffy, IRE Headquarters, 1 East 79th Street, New York City.

contributors

R. C. Howard (SM'48–A'54) was born in Manhattan, Kans. on June 6, 1923. He was graduated from Whitman College in 1944 with the A.B. degree in physics and mathematics.

After graduation and a two year period in the U. S. Navy, he returned to Whitman College as a physics instructor. He received the M.S. degree in electrical engineering from the California Institute of Technology in 1950. After a year of graduate study at the Imperial College, University of London, he returned to the California Institute, where he received the Ph.D. degree in June 1953. During the summers he was employed at USNOTS, China Lake, Calif., as an electronics engineer.

Since February 1953, Dr. Howard has been a member of the technical staff of the Bell Telephone Laboratories, New York, N. Y. He is a member of Sigma Xi and Phi Beta Kappa.

Samuel Lubkin (SM'46) received his B.S. in Electrical Engineering from Cooper Union in 1927, his M.S. in Mathematical Physics from the University of Chicago in 1928, and his Ph.D. degree in Applied Mathematics from New York University in 1939. In 1944 he received an E.E. degree from Cooper Union. For ten years he was an engineer with the Otis Elevator Company, and Director of the Inspection Laboratory of the Signal Corps for six years.

Dr. Lubkin has been in the digital computer field since 1946. Since then he has been associated with the Ballistics Research Laboratories, the Reeves Instrument Corporation, the University of Pennsylvania, the National Bureau of Standards, and the Electronic Computer Corporation. His assignments have included work on the ENIAC, EDVAC, SEAC, and the ELECOM computers. Dr Lubkin is now Director of the Electronic Computer Division of Underwood Corporation.

He is a member of the Association for Computing Machinery, the American Association for the Advancement of Science, and the Institute of Electrical Engineers.

David E. Muller was born in Austin, Texas on November 2, 1924. He received the B.S. degree in 1947 and the Ph.D. in 1951 from the California Institute of Technology, where he stayed for an additional year as a Research Fellow.

Dr. Muller has been associated with the Digital Computer Laboratory of the University of Illinois since 1952 as University Fellow and Research Assistant Professor of Applied Mathematics. He is working on applications of Boolean algebra and digital computer programming techniques.

Dr. Muller is a member of the American Physical Society, American Association for the Advancement of Science, and Sigma Xi.

E. C. Nelson was born in Starbuck, Minn., in 1917. He received the B.A. degree in 1938 from St. Olaf College, Northfield, Minn., and the Ph.D. degree in 1942 from the University of California.

In 1942–43 he was an instructor in physics, and research associate in the Radiation Laboratory, University of California; 1943–46, Group Leader with the Theoretical Physics Division, Los Alamos Laboratory; 1946–47, Assistant Professor at the University of Chicago; 1947–48, partner in Frankel and Nelson, consultants in mathematical physics; since 1948, Head of Advanced Electronics Laboratory, Hughes Research and Development Laboratories, Culver City, Calif.

He is a member of Phi Beta Kappa and Sigma Xi, and a recipient of the University of California's Whiting Fellowship.

Lazarus G. Polimerou (S'50–A'53) was born in Glens Falls, N. Y. on January 28, 1929. He received the B.S.E.E. degreee in 1952 from Northeastern University. He began working for USN Underwater Sound Laboratory, New London, Conn. as a co-op student in January, 1951. While there he participated in the development of a sonar system, later testing and evaluating U. S. Navy contract equipment.

Mr. Polimerou joined U. S. Ordnance's Electro-Mechanical Laboratory Division at White Sands Proving Ground, N. M., in June, 1952, where he developed a new function generator design while working in the Servo-Computer Branch as project engineer. There he participated in placing into operation the analog computer program. He was a member of the staff assigned to the solution of rocket trajectories and other guided missile problems. Later he was made responsible for the Analog Computer Group of the Computer Section, EMLD. In July, 1953, he entered the U. S. Army and was assigned to the Signal Corps Engineering Laboratory at Ft. Monmouth, N. J. as an instructor for a new Equipment Introductory Team. He was then transferred to White Sands Proving Ground, where he is presently engaged as an engineer with The Analog Computer Section of Dynamic Systems Branch, EMLD.

Mr. Polimerou is an associate member of the American Institute of Electrical Engineers.

R. D. Ryan (S'47–A'49) was born on January 5, 1925, in Sydney, Australia. He received the B.Sc. degree in physics, and the B.E. degree in mechanical and electrical engineering, from Sydney University, in 1946 and 1948 respectively.

Since graduating, Mr. Ryan has worked as a Research Officer in the Radiophysics Division of the Australian Commonwealth Scientific and Industrial Research Organization. He was engaged on the development of test equipment, input and output devices, and a mercury delay-line memory unit for the CSIRO computer. He has recently transferred to work on semi-conductor devices.

C. J. Savant, Jr. (S'52–A'53) was born in Butte, Mont. on August 9, 1926. He received the B.S. degree in electrical engineering in 1949, and the Ph.D. degree in 1953, from the California Institute of Technology.

From June 1951, he worked part-time as a research engineer at the Jet Propulsion Laboratory. Completing his work for his doctorate in January 1953, he joined the Research and Development Laboratories of North American Aviation, New York, N. Y., as a senior research engineer. He has been concerned with systems engineering, servomechanisms, and computers.

Dr. Savant also holds a Visiting Assistant Professor rank at the University of Southern California, where he teaches graduate night courses in Advanced Servomechanism and Circuit Analysis. He is a member of Tau Beta Pi, and Sigma Xi.

R. Zweizig (S'47–A'49) was born in Zion, Ill. in 1923. He received the B.S. degree in electrical engineering from Northwestern University in 1948. After graduation he joined the Department of Psychology of Northwestern University where he was concerned with the design of special research instruments.

Since 1951, he has been with the Jet Propulsion Laboratory of the California Institute of Technology and is a Research Engineer in the Instrument Development Section.

He is a member of the American Association for the Advancement of Science and is currently a graduate student at UCLA in addition to his work at the Jet Propulsion Laboratory.

Review Section

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. All articles and books reviewed are numbered sequentially for each year; where known, the Universal Decimal Classification number is also given. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.

H. D. Huskey, Editor

GENERAL

54-113

Introducing Computers to Beginners—Geoffrey Ashe. (*Computers and Automation*, vol. 3, pp. 8–11; March, 1954.) This article contains sound advice for the teacher of an introductory course on computers who needs to remove himself from the perspective of one thoroughly familiar with computers in all their intricate detail, and present his wealth of information in a form that can be assimilated by his uninitiated audience. The author draws directly from his experience as a student at the Wayne University seminar on machine computing, Summer, 1953, to point out several specific areas of obscurity in the presentation of course material. His advice: Start slowly from the beginning; explain what is meant by digital coding and transmission of information; always relate operating programs to actual happenings inside the computer; use elementary (to the student, not to the computer) examples, at first; use visual aids that are more dynamic than the usual block diagram; set precepts down clearly with concrete illustrations as to how they might be carried out. Surely the future students of those who read this article will experience some of the delight in the clarity of exposition of the course material that their teachers will have experienced in reading the article and heeding the author's recommendations.

G. E. Gourrich

54-114

A Glossary of Computer Terminology—Grace M. Hopper. (*Computers and Automation*, vol. 3, pp. 14–18, 20, 22; May, 1954.) "This glossary has been assembled from the point of view of applications not that of engineering. It is mainly a UNIVAC vocabulary, although some attempt has been made to make it applicable to all computers." This glossary of over 150 terms and phrases, borrowed in part from presently printed material, such as the "IRE Standard on Electronic Computers: Definitions of Terms," and the "Glossary" published by *Computers and Automation*, is a comprehensive carefully written set of definitions of words and phrases in the programmer's language used in describing routines, methods of programming, and machine operation. (See 54-115 of this issue.)

G. E. Gourrich

54-115

Glossaries of Terms—More Discussion—Nathaniel Rochester, Willis H. Ware, Grace M. Hopper, E. C. Berkeley, and others. (*Computers and Automation*, vol. 3, pp. 21–24; March, 1954.) Reprints from other publications describe: (a) The work being done by the Eastern and Western Definitions Subcommittees of the Electronic Computers Committee of the IRE in compiling a second IRE glossary of computer terms to be published before the spring of 1955. (b) The "glossary of Computer Terminology" published by Remington Rand, Inc. E. C. Berkeley provides several questions and answers showing the specific differences in character between these works and the dictionary being compiled by Computers and Automation, concluding that there is a continued need for the work being carried out by Computers and Automation utilizing an approach which produces a more inclusive dictionary more rapidly, if not as perfectly, than the former works. (See 54-114 of this issue.)

G. E. Gourrich

621.385.2 54-116

Computers and Automata—Claude E. Shannon. (*Proc. I.R.E.*, vol. 41, pp. 1234–1241; October, 1953.) This is a provocative article dealing with aspects of automatic computers other than those of numerical computation. An introduction to current experiments in this field is provided. In addition, some interesting speculations are advanced concerning future developments in machines to solve problems in logic and to play games, and in machines that are capable of adaptation (or learning) and self-reproduction. A number of interesting references to the subject of computers for non-numerical purposes is given in the bibliography.

E. L. Braun

54-117

The Concept of Thinking—Elliot L. Gruenberg. (*Computers and Automation*, vol. 3, pp. 18–21; April, 1954.) Searching for a definition of thinking which is useful in the design and application of machines for automation, the author points out in many examples that each particular group of scholars producing a definition has been interested in explaining the thought process from that particular viewpoint which best illustrates or explains specific phenomena in which the group is interested. Many such viewpoints are briefly described, and the resulting explanations of thought are given, together with some of the disadvantages of these definitions as applied to the study of automation. It is pointed out that the pragmatic philosophers, John Dewey in particular, provide the most useful definition of thinking as it applies to automation: "an operation in which present facts suggest other facts and induce belief in the suggested facts on the ground of the real relation in the things themselves." Thus, it is concluded that Dewey's definition appears to be the clearest statement of the thinking function which a search of science and the philosophy of human understanding can uncover.

G. E. Gourrich

681.142 54-118

Über die Grundzüge eines Programms für eine schachspielende Rechenmaschine or On the Fundamental Features of a Program for a Chess-playing Computer—G. Schliebs. (*Funk und Ton*, vol. 7, pp. 257–265; May, 1953.) This article is essentially a translation into German of "Programming a Computer for Playing Chess," C. E. Shannon, *Phil. Mag.*, Ser. 7, vol. 41, pp. 256–275; 1950. A numerical evaluation function is defined for a chess position and the machine is programmed to perform the minimax calculations of game theory with respect to this function for an n move strategy. An improved strategy in terms of a stability function is also briefly considered. The evaluation function, the nature of the stability function, and all the details of the program are identical with those suggested by Shannon. Since in each case these were only tentative suggestions and did not represent the only possible description, it is clear that the article was intended solely for the benefit of German readers who might have difficulty reading Shannon's article in English. In addition to reproducing all the important features of Shannon's work, this article also includes a slight error which was present in the earlier paper. The total number of possible moves in a chess game is given as 6350 (bearing in mind the 50 move draw rule). This number should be reduced by 400 since a minimum of 4 pawn captures on each side is necessary to allow all the pawns to promote. It is regrettable that the author did not at least trouble to improve some of Shannon's estimates of the computing time required. These are much too optimistic even for the fastest of present day computing machines. It is even more regrettable that the author did not acknowledge the priority of Shannon's work other than listing it as one of the references.

E. Levin

54-119

Towards More Automation in Petroleum Industries—Sibyl M. Rock. (*Computers and Automation*, vol. 3, pp. 6–7, 16; March,

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—*The Editor*

1954.) Compact displays presenting 2000 or more measurements of secondary variables are now used in process control. Usually the variables measured are not the actual products but some related physical characteristics. End-point checks of actual composition of the product are also necessary for complete control. "The problem of large-scale automation using both intermediate and end-point analysis is being attacked from two sides. One is monitoring and display of one or perhaps more indicators of composition, such as a mass spectrum peak or an infrared absorption at a specified wave length. Here the sampling variables and time lag can be minimized. Second, mixtures of greater range and complexity are being analyzed, and the computations required for their solution are being mechanized." Extending the first approach to more components, and simplifying the instruments required for the second, will lead to continuous analyses with automatic feedback to the controllers, eliminating much of the human intervention now necessary. Humans will still be required to cope with unforeseen conditions.

G. E. Gourrich

54-120

The Foundations of Computing Machinery, Part II—John D. Goodell. (*Jour. Computing Systems*, vol. 1, pp. 86–110; January, 1953.) This article is a continuation of the author's introductory discussion of the theory of decision elements for computer logic together with a brief discussion of the magnetic decision elements already produced. Methods for recognizing such logical functions as negation and dual are given and a substantial discussion of elementary circuit synthesis is included with many examples. Unfortunately, their value as orientation in computer design is limited by the fact that 80 of the 84 designs disregard timing problems. This inattention to timing and similar problems of physical realization apparently has led to the somewhat misleading statement (p. 89) "there are four universal elements (S, D, C, L) from any one of which a complete system can be constructed." This statement is confusing in two respects: 1. The two Sheffer functions (S and D) are not universal unless supplemented by a delay element. (cf. The author's "Notes on Decision Element Systems Using Practical Techniques," *op. cit.*, vol. 1, p. 197; July, 1953. A similar result can be rigorously proved for arbitrary radix.) 2. If clock pulses can be used as input, H and T (the negations of C and L respectively) are also universal as is shown by this reviewer in "On Completeness of Decision Element Sets," *Jour. Computing Systems*, vol. 1, pp. 150–154; July, 1953. The article provides a good introduction to many problems of logical design for beginners and decision element terminology and notation for those in the field not familiar with them.

Norman M. Martin

54-121

On a Universal Decision Element—Boleslaw Sobocinski. (*Jour. Computing Systems*, vol. 1, pp. 71–80; January, 1953.) The author raises the question of the existence of a decision element (circuit) which, by alternative wirings at the input, will be able to produce any radix two decision element of two inputs and one output. This is equivalent to the problem in classic propositional logic of finding a function f such that any two-place function can be expressed by a formula consisting of the sign for f with either propositional variables or constants (but no nonconstant functions) in the argument places. (Constants are allowable because of the possibility of realizing them respectively by connection with the clock or with nothing.) Sobocinski shows that no such function exists with 3 arguments but that the function of 4 arguments, expressible in the notation of *Principia Mathematica* as:

$$p \equiv \cdot p \equiv r \cdot q \equiv s$$

has the desired property. No discussion is given of the physical realization of the corresponding 4-input decision element. This reviewer believes that such a circuit can be designed using 6 magnetic cores and approximately 20 diodes. It would probably have twice the delay of magnetic decision elements currently available.

Norman M. Martin

621.375.2×510 54-122

Elements of Boolean Algebra for the Study of Information-Handling Systems—Robert Serrell. (*Proc. I.R.E.*, vol. 41, pp. 1366–1380; October, 1953.) This paper explains the algebra of classes and shows how this subject may be applied to the study of logical nets without delays. A number of formulas which are useful in the analysis and synthesis of logical nets are presented: formulas for complementation, distribution, reduction to normal form, etc. The principle of duality and its uses are developed in some detail. A procedure for finding the simplest (disjunctive or conjunctive) normal form of a formula (by listing all the possible terms that enter into its normal forms) is described and illustrated. Finally, the material of the paper is applied to the analysis, synthesis, and minimization of a binary adding circuit. The exposition is in general good, and the development sufficiently rigorous for the author's purpose. The main weakness of the paper stems from the fact that the algebra of classes is not as well suited for the study of nets as is the propositional calculus. That this is the case may be seen by considering the kind of connecting link required in each case. Let a be a wire which may be either energized or not. The following *sort* of interpretation is required for using the calculus of classes to study nets: A is the universal class if a is energized, otherwise A is the null class. For the application of the propositional calculus to nets we need only let "A" be the sentence "a is activated." The latter connection is more natural and direct than the former, and hence easier to make. Moreover, since in the application of the calculus of classes to nets a universe of discourse consisting of only two distinct classes (the universal class and the null class) is needed, all of the theorems of interest for this application may be stated without quantifiers and hence can be established by three very useful procedures: truth table methods, natural deduction techniques, and convenient combinations of these. (See Irving M. Copi, *Symbolic Logic*, pp. 27, 42 and 64 respectively, for a presentation of these procedures.) But because these procedures have been developed in connection with the propositional calculus their applicability to the part of the calculus of classes needed for the study of nets is likely to be overlooked (as is indeed largely the case in the present article).

Arthur W. Burks

54-123

The Recognition and Identification of Symmetric Switching Functions—S. H. Caldwell. (*Communication and Electronics*, No. 12, pp. 142–147; May, 1954.) A certain class of switching functions, known as "m out of n" types, lends itself to simpler switching circuits than the straightforward series-parallel arrangements. When one or more of the input variables is inverted, the same simplifications can be achieved, but the recognition of the true nature of the situation becomes much more difficult. This paper presents a map method of recognizing and identifying all forms of this class of functions, known as symmetric functions. The map is limited to functions of four variables although means for handling more than four variables are explained. Discussions of the paper by S. H. Washburn, M. Karnaugh, and S. H. Caldwell are appended.

R. K. Richards

54-124

Digital-to-Analog Shaft-Position Transducers—S. J. O'Neil. (*Communication and Electronics*, No. 5, pp. 37–41; March, 1953.) The principles involved in converting from a digital representation to the analog voltages necessary for the control of a synchro motor are discussed. Circuits are shown both for 2-phase and 3-phase units. Discussions are included concerning the achievable accuracy with various arrangements including the use of torque amplification as obtained from a servomechanism system. Photographs of an assembled transducer are included although no data about this unit are given.

R. K. Richards

54-125

Roster of Organizations in the Field of Computers. (*Computers and Automation*, vol. 3, pp. 8–16; April, 1954.) With information as of March 10, 1954, this roster reports organizations making or developing computing machinery, systems, data handling equipment, or equipment for automatic control and material handling. Each complete roster entry contains: name of the organization, its address, nature of its interest in this field, kinds of activity it engages in, main products in this field, approximate number of employees, year established, and a few comments and current news items. Not all of the organizations listed have supplied the information in their listing for the roster. There are about 200 listings.

G. E. Gourrich

ANALOG COMPONENT RESEARCH

681.142:621.376.22 54-126

Instantaneous Multiplier for Computers—M. Mehron and W. Otto. (*Electronics*, vol. 27, pp. 144–148; February, 1954.) Two voltage functions can be instantaneously multiplied by the electronic multiplier described in this article. The input signal may be complicated wave-forms, but the fre-

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—*The Editor*

quency components contained are limited to the range of from 0 to 5000 cps. The unit will multiply dc voltages. The multiplying process consists of combining a crystal controlled carrier frequency, and the two input voltages by means of two balanced modulators. This resultant signal and the carrier frequency are passed through a phase sensitive detector. The output of the detector represents the product of the input signal with the proper sign. That is, if the input signals are of the same polarity the output will be positive, but if of different polarities the output will be negative. The highest frequency component this equipment will multiply is about one per cent of the carrier frequency used (456kc). The authors claim that input frequency of several megacycles may possibly be multiplied by using a much higher carrier frequency.

Norman F. Loretz

54-127

An Analog Computing Circuit for the Evaluation of the Ratio of Two Slowly Varying Potentials—R. L. Gordon. (*Jour. Sci. Instr.*, vol. 31, pp. 166–169; May, 1954.) An electronic circuit is described which accurately computes the ratio of two steady or slowly varying potentials and displays the result as a meter deflection. It also can compute reciprocals and products. Feedback is used to reduce the circuit's sensitivity to variations in tube characteristics, and an accuracy of better than 1 per cent of full-scale deflection of the meter has been obtained over a wide input range. The circuit can rival the accuracy of the best servo mechanisms and operates considerably faster than a mechanical servo. One of its applications is the monitoring of radiation sources.

A. J. Dowling

681.142 54-128

Application Factors for Electrical Resolvers—S. Davis. (*Elect. Mfg.*, vol. 51, pp. 128–133, 326, 328; March, 1953.) The device described resembles a small motor and was originally designed for solving trigonometry problems in conjunction with analog computers. Possible applications for control purposes in industry are discussed.

Courtesy *Proc. I.R.E.* and *Wireless Engineer*.

ANALOG EQUIPMENT

681.142 54-129

A New Analog Computer—E. L. Thomas. (*Engineering* (London), vol. 176, pp. 477–479; October, 1953.) A general-purpose computer of differential-analyzer type, designed for economic quantity production, is described. Three basic elements are used, viz., (a) scaling units, essentially 3-decade variable resistors, (b) function units comprising RC networks, (c) high-gain amplifiers. Facilities for cro and graphical display are provided.

Courtesy *Proc. I.R.E.* and *Wireless Engineer*.

54-130

A General Purpose Electronic Analog Computer—(*Engineer, Lond.*, vol. 196, pp. 395–397; September, 1953.) The electronic analog computer described is a general-purpose equipment designed for economical quantity production. It is a differential analyzer and its capacity is such that three similar computers coupled together should be capable of handling a general six-degrees-of-freedom problem. Some typical aircraft design applications are indicated in the article. Courtesy of *Applied Mechanics Reviews*.

54-131

An Automatic Analog Computer for the Solution of Mine Ventilation Networks—D. R. Scott and R. F. Hudson. (*Jour. Sci. Instr.*, vol. 30, pp. 185–188; June, 1953.) The distribution of air in a mine catacomb is expressible as the solution of a system of algebraic equations, the variables always appearing as squares. The author suggests an electrical analog that is obtained by introducing a variable resistance proportional to the current across it. The resistance value is set by a servo, nulling on current. The authors describe in some detail the differential relay that acts as the current comparator unit of the device they have developed.

Paul Brock

UTILIZATION OF ANALOG EQUIPMENT

681.142 54-132

General Survey of the Operating Principles of Electrical Analog Computers—C. Mounier. (*Rev. Gén. Élect.*, vol. 62, pp. 515–530; November, 1953.) A survey with particular reference to computers constructed by the Société d'Electronique et d'Automatisme; difficulties encountered in studying the accuracy of these machines are discussed.

Courtesy *Proc. I.R.E.* and *Wireless Engineer*.

621.385.2×510 54-133

The Solution of Partial Differential Equations by Difference Methods Using the Electronic Differential Analyzer—Robert M. Howe and Vincent S. Haneman, Jr. (*Proc. I.R.E.*, vol. 41, pp. 1497–1508; October, 1953.) The principles of the electronic differential analyzer are discussed briefly. Its application to the solutions of three partia differential equations is then considered. The three equations are those of heat flow, wave motion, and vibrating beams. In each instance, the spatial difference equation is derived, the corresponding computer circuit is indicated, and, finally, a comparison is made of the solution so obtained with the analytical solution of the differential equation. In the main, the discussion is concerned with only one spatial dimension, although there are some remarks on the two dimensional, heat flow equation. Two types of vibrating beams are considered, namely, the cantilever and the hinged-hinged variety. The presentation is very clear and simple and instructive. It would have been useful to include some remarks of a practical nature on the authors' experiences with the actual circuitry, such as an account of any experimental difficulties, and the sort of times involved to prepare the circuits and to obtain solutions. It would thus have been possible to make comparisons with other approaches, in particular, purely digital schemes.

N. Metropolis

621.3752×388×R143 54-134

Economic Analogs—Otto J. M. Smith. (*Proc. I.R.E.*, vol. 41, pp. 1514–1519; October, 1953.) This paper presents four economic systems in which electric and electronic analogs can be used for economic system study. Several economic problems falling into the class of n equations in n unknowns are discussed under the section "Linear Static Unilateral Analog." A distinction between the unilateral (or cause-and-effect) analog and the bilateral (a closed-loop system) analog is clearly presented. The example used to illustrate a Dynamic Bilateral System is the classic example of the study of inventory oscillations. An electrical network utilizing R, L, C, diodes, and voltage sources is used to illustrate a simple model of this problem. A block diagram showing a Dynamic Unilateral System (a production analog) is adequately described. This problem can be set up on any of the general purpose analog computers commercially available. A very interesting example of a plant which produces all capital goods is block diagramed. A short discussion of economic problems related to international and domestic trade is presented under the title of "Decision Function Network." The author points out that economists must become skilled in the use of the mathematical tools used by engineers working in the servomechanisms and system-design field. The analogs do not relieve the problem of obtaining accurate data but they can point the way as to which economic data should be gathered in the economic system under study. The paper clearly shows that analog computers have utility in the economic field. An excellent bibliography has been compiled and will be a great aid in obtaining a background in this interesting application of analog computers.

Raymond Davis

DIGITAL COMPONENT RESEARCH

681.142:621.385 54-135

Valve Reliability in Digital Calculating Machines—L. Knight. (*Electronic Eng.*, vol. 26, pp. 9–13; January, 1954.) This article summarizes measures which can be taken to reduce the number of tube failures and the inconvenience of unscheduled maintenance in digital computers. Measures discussed include choice of tube type for long life, use of conservative ratings, use of wide tolerances in circuit design, individual testing of tubes, testing the complete machine, preventive maintenance, and facilities for rapid servicing.

R. G. Canning

54-136

Type-7 Crossbar Selector—R. W. Hutton. (*Communication and Electronics*, No. 10, pp. 830–833; January, 1954.) The functioning of the Type-7 crossbar selector is explained. Circuits are shown to illustrate how the crossbar selector, together with relays, magnetic counters, and other components, can be used to select a line in a dial telephone switching system.

R. K. Richards

54-137

A Cold Cathode Batching Counter—P. E. Tooke. (*Electronic Eng.*, vol. 26, pp. 160–162; April, 1954.) An industrial counter for batching steel components in preselected batches, at speeds up to 200 com-

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—*The Editor*

ponents per second. Tubes used have maximum counting rate of 550 per second.

R. G. Canning

54-138

A Cold-Cathode Scaling Unit—C. D. Florida and R. Williamson. (*Electronic Eng.*, vol. 26, pp. 186–190; May, 1954.) Introduction to article states: A new scaling unit is described which uses cold-cathode decade scaling tubes, coupling between stages being performed by cold-cathode gas-filled triodes. The unit is slow compared with vacuum tube scaling units, but its 500 μsec. resolving time makes it suitable for nearly all applications using Geiger Muller counter tubes as detecting elements. For those applications, the new scaler is simpler and should be cheaper and more reliable than existing types.

R. G. Canning

54-139

Decimal Counting Tubes—K. Kandiah. (*Electronic Eng.*, vol. 26, pp. 56–63; February, 1954.) A survey of currently available types of counting tubes (primarily British) with emphasis on some of their limiting characteristics. Tube types include: glow-discharge using ten independent cathodes and one anode in gas-filled envelope, CRT with electrostatic focusing and deflection, and the trochotrons using heated cathodes and electron beam in crossed electrostatic and magnetic fields. Minimum resolving times in microseconds are: first type, 250; second type, 30; third type, 5.

R. G. Canning

54-140

A Magnetic Impulser—C. A. Routledge. (*Electronic Eng.*, vol. 25, pp. 118–119; March, 1953.) A device to replace conventional circuit breakers in punched card reading circuits is described. The device has advantages for use in higher speed machines, for use with more sensitive relays, for input to electronic computer circuits (avoiding the problem of contact bounce found in conventional circuit breakers), and for longer life under higher operating speeds. It consists of a serrated timing wheel that passes between the poles of two sets of pick-up coils, which in turn are supplied from an energizing coil. A sharp impulse is obtained as a "tooth" of timing wheel enters the gap between the poles of the pick-up coils; the reverse polarity impulse obtained when the tooth leaves the gap is ignored. A pulse to space ratio of 1 to 2 and 1 to 3 is obtainable.

R. G. Canning

54-141

Ferroresonant Flip-Flop Design—Rudolph W. Rutishauser. (*Electronics*, vol. 27, pp. 152–153; May, 1954.) The physical and practical applications of ferroresonant flip-flops are dealt with in this article. Schematic diagrams of a flip-flop unit and a five-stage ring counter are shown. An explanation of the operation of both the flip-flop and the ring counter is given. The author states that when using $\frac{1}{8}$ mil 4-79 MO-Permalloy as the core material and an ac generator frequency of about 1.3 mc, flip-flops have been triggered at a rate exceeding 100 kc. A reference is made to an earlier article by Carl Isborn in the April, 1952 *Electronics* which presents a detailed operation of the ferroresonant units.

Norman F. Loretz

54-142

A Graphical Method for Flip-Flop Design—R. F. Johnston and A. G. Ratz. (*Communication and Electronics*, No. 5, pp. 52–56; March, 1953.) The basic Eccles-Jordan flip-flop circuit is discussed with particular emphasis on the factors which contribute to stability. Design criteria are set forth and a graphical means is explained for determining the range of resistor values and supply voltages which will yield a stable circuit. Attention is centered on the steady-state conditions and transition time, and no information about amplitude and duration of the input pulse is presented. Two sample problems are worked out.

R. K. Richards

54-143

Multiplication in the Manchester University High-Speed Digital Computor—A. A. Robinson. (*Electronic Eng.*, vol. 25, pp. 6–10; January, 1953.) A description is given of the multiplication method used in the electronic digital computer built by Ferranti and installed at Manchester University. Binary multiplication essentially consists of many additions; these can be done at a slow rate of speed in a single adding circuit, at a high speed by the use of many adding circuits, or at an intermediate speed by the use of an intermediate number of adding circuits. It is this last named principle which is used in the Manchester machine. Multiplication of two 40-bit numbers is accomplished in 3.36 milliseconds, or about three add times. The multiplier is separate from the accumulator, and the results of the multiplication can be added to or subtracted from previous results standing in the accumulator. The multiplier unit contains some 250 pentodes and 700 diodes, out of a total of 1700 pentodes and 2300 diodes in the machine.

R. G. Canning

54-144

Principles of Tape-to-Card Conversion in the AMA System—W. B. Groth. (*Communication and Electronics*, No. 5, pp. 42–52; March, 1953.) The conversion from 28-hole paper tape to standard IBM punched cards for the AMA (automatic message accounting) system is described in considerable detail. The AMA system is reviewed. Considerable attention is given to the arrangement of the information on the input tape and the output cards.

R. K. Richards

54-145

The Diode Matrix as a Component in Relay Switching Circuits—G. L. Bush. (*Communication and Electronics*, No. 10, pp. 833–838; January, 1954.) An application of selenium rectifiers in the energizing of relays is described. The basic problem was in the address circuits of a magnetic drum used for storing stock market quotations. Through the use of a dial system a broker may obtain bid-and-asked quotations for the desired stock in an automatic fashion. In addition to a brief description of the entire machine, the diode circuits are presented along with a comparison of the amount of relay equipment required to perform the same switching functions without the diodes. Test equipment for the diode matrix is also described.

R. K. Richards

54-146

Quarterly Report No. 1, Second Series—John R. Bowman, F. A. Schwertz, et al. (*Quart. Prog. Rept. Computer Components Fellowship Mellon Inst.*, 135 pp.; October 1, 1953 to December 31, 1953.) Sections I and II of this report comprise a discussion of two new storage devices. The first is a bistable vacuum diode containing a photocathode and a phosphoranode which may be switched from one state to the other by means of a pulse of light; the second, a gas-filled diode which may be transferred from the conducting to the nonconducting state, and vice versa, by an rf pulse. For the first device the transition from the "off" to the "on" state is presently effected by a weak pulse of light and transition in the reverse direction by a strong pulse of light. In principle, however, the device may be transferred from either state to the other by means of a light pulse of carefully controlled width and amplitude, that is, it may be made to count light pulses. The gas (neon) diode is an analog of the photodiode, the rf pulse in the former playing the same role as the light pulse in the latter. It differs in the fact that the time required to place the diode in the conducting state (firing time) is much shorter than the time required to place it in the nonconducting state (deionization time), whereas in the case of photodiode the time required to switch to either state is the same. Section III contains a summary account of some experiments in which saturable ferromagnetic ferrites were employed for pulse-switching and gating purposes. This section has been prepared in a form suitable for formal publication. Experiments pointed toward the adaptation of the Xerographic printing process to the production of printed circuits is discussed in Section IV. Some preliminary experiments relative to the ac behavior of nonlinear semiconductor resistors are discussed in Section V. The behavior of an "and circuit" containing nonlinear resistor switching elements is analyzed in terms of the results of these experiments.

F. A. Schwertz

54-147

Quarterly Report No. 2, Second Series—John R. Bowman, F. A. Schwertz, et al. (*Quart. Prog. Rept. Computer Components Fellowship Mellon Inst.*, 105 pp.; January 1, 1954 to March 31, 1954.) The report consists of six separate sections. A summary of the content of each section follows. Section I comprises a discussion of techniques for making electroluminescent light sources. Of particular importance is a description of a method for the production of self-luminous halftones in which the Xerographic (dry) printing process is employed to control the distribution-in-density of the electroluminescent powder. A three binary digit adder which was materialized by applying printed circuit techniques to a ceramic-bonded sheet ($3'' \times 3'' \times 1/16''$) of silicon carbide is described in Section II. Section III has mostly to do with the details of a vacuum system designed specifically for ultra-high vacuum work. Pressures of 10^{-8} mm of Hg and lower are obtainable. Section IV constitutes a progress report on a project aimed at producing printed circuits with the aid of the Xerographic printing process. Although the prospect of producing printed circuits by

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—*The Editor*

this means appears promising, no circuits have been printed successfully up to the present time. Section V on "Saturable Transformers as Gates" is an exact duplicate of a manuscript which has been submitted for journal publication. Section VI contains a discussion of some preliminary experiments aimed at the production of "linear resistor blanks." The reaction of stannic chloride with glass substrates at elevated temperatures is employed to materialize the resistors on the glass blanks.

F. A. Schwertz

54-148

Measuring the Accuracy of Magnetic Delay Units—G. Jamieson. (*Electronic Eng.*, vol. 26, pp. 203–205; May, 1954.) A description is given of a Time Interval Marker, a unit which provides trains of accurately spaced negative pulses, and its use in estimating the accuracy of time delays obtainable with a recording system. The pulse trains are of 1 millisecond, 10 ms, and 100 ms periods, and a "ruler" type display is provided.

R. G. Canning

54-149

The Single-Core Magnetic Amplifier as a Computer Element—R. A. Ramey. (*Communication and Electronics*, No. 4, pp. 442–446; January, 1953.) It is shown how certain logical components for computers can be developed from the single-core magnetic amplifier. Circuits are shown for coincidence units, ring counters, and flip-flops. An experimental assembly involving units of each of these categories was constructed, and its performance is reported. The assembly which was described operated at only 60 cps but the possibilities for higher speed operation with appropriate modifications in components were pointed out.

R. K. Richards

54-150

A Review of Magnetic and Ferro-electric Computing Components—V. L. Newhouse. (*Electronic Eng.*, vol. 26, pp. 192–199; May, 1954.) This review is aimed at correlating and systematizing the different lines of approach for memory and logical units in digital computers. It discusses regenerative delay lines, magneto-striction delay lines, magnetic drums and other nonregenerative delay lines, the magnetic counter, tube and magnetic shift registers, magnetic core storage, magnetic core switching circuits, and ferro-electric developments. Some comments on future developments are included. The article makes note of several as-yet-unpublished contributions, and includes a 25-reference bibliography.

R. G. Canning

54-151

Ferroelectric Materials as Storage Elements for Digital Computers and Switching Systems—J. R. Anderson. (*Communication and Electronics*, No. 4, pp. 395–401; January, 1953.) Single crystals of barium tetanate, which have a reasonably rectangular hysteresis loop, have been studied for possible application as computer storage elements. The properties of the crystals are described in some detail, and the basic storage mechanism is described. Various storage systems, shifting registers, and arrays are suggested. A few preliminary experiments to test the feasibility of the storage circuits have been performed.

R. K. Richards

54-152

Ferrite Memory Devices—Ephraim Gelbard and William Olander. (*Computers and Automation*, vol. 3, pp. 6–7, 13, May, 1954.) This is a very brief and quite complete introductory description of ferrites. Composition and physical properties are described. Magnetic characteristics and how these may be utilized in storing digital information are described, first for the storage of one bit of information and leading into applications of many ferrite cores arranged in a three-dimensional set of planes as large-scale high-speed memory devices. Here the article may have omitted sufficient detail for the uninitiated reader. Magnetic core storage may be constructed in units of as much as 16,384 words of storage per plane, having an access time of 3–6 microseconds. Occupying a space of about 1/10th square inches per bit, a core storage plane requires approximately $2\times\sqrt{}$ total number of bits per plane electronic current sources to drive the ferrite cores. There is no known deterioration with age and usage.

G. E. Gourrich

54-153

Nondestructive Sensing of Magnetic Cores—D. A. Buck and W. I. Frank. (*Communication and Electronics*, No. 10, pp. 822–830; January, 1954.) A system is described for the nondestructive sensing of information stored in magnetic cores. The sensing field is applied at right angles to the stored field. Because the stored field is in a direction of easy magnetization and because the magnitude of the sensing field is limited, the core will revert to its original state when the sensing field is removed. The polarity of the output signal is dependent upon whether a "one" or a "zero" was stored in the core. Methods of obtaining the quadrature fields are described. The results of experiments are reported, and it has been found that the action is fast with output signals being obtained which have a duration of 0.2 μsec. Also, output voltages in excess of 1 volt per turn have been achieved. The results of endurance tests involving up to 1,200,000,000 readouts are given.

R. K. Richards

DIGITAL EQUIPMENT

54-154

An Industrial Batching Counter—R. W. Brierley. (*Electronic Eng.*, vol. 26, pp. 157–160, April, 1954.) A counting equipment is described which controls the batching of mass-produced articles into small pre-determined quantities. Cold-cathode counters are used; input filter circuits limit counting rate to 25 counts per second. Unit discussed accumulates up to 199 pulses.

R. G. Canning

54-155

A Subscriber Toll Dialing Tape Reader—W. H. Blashfield. (*Communication and Electronics*, No. 5, pp. 17–21; March, 1953.) A machine is described which computes charges and prints toll tickets from the information contained in punched tape that was prepared by a dial telephone system. The machine is intended for use in relatively small systems, and will print tickets for 300 telephone calls in approximately 45 minutes. The computing circuits contain 10 tubes and a number of relays (See 54-46.)

R. K. Richards

54-156

Automatic Testing of Wired Relay Circuits—A. N. Hanson. (*Communication and Electronics*, No. 10, pp. 850–857; January, 1954.) A flexible machine for testing wired relay circuits automatically and at high speed is described. Connections to the circuit under test are made through the use of a perforated paper tape containing 28 rows of holes. Tests are made at the rate of 16 per second. The preparation of a new tape is all that is required to adapt the machine to the testing of a new relay circuit. The circuits used in the tester and the means for applying supply voltages and testing conditions to the multiplicity of points in the circuit under test are explained in some detail.

R. K. Richards

54-157

A Fully Automatic Teletypewriter Switching Center for Military Use—L. Johnston and R. C. Stiles. (*Communication and Electronics*, No. 11, pp. 27–37; March, 1954.) This paper explains many of the problems peculiar to switching in a teletypewriter system. Among these problems are the storing of messages on tape, the automatic selection of routing circuits from characters recorded on the tape, multiple-address messages, and the checking for missing messages. In a military installation there are also the problems of priority messages and the need for sudden and extensive reorganizations of the network. The equipment installed to accomplish these and other functions in an automatic fashion at the Fifth Army Headquarters in Chicago, Illinois, is described. Photographs of some of the units and components, a block diagram of the system, and some of the basic circuits are presented.

R. K. Richards

54-158

High-Speed Teletypewriter Equipment for the Armed Services—C. E. Schultheiss. (*Communication and Electronics*, No. 11, pp. 88–93; March, 1954.) A new teletypewriter mechanism capable of 60 to 100 word-per-minute operation is described.

R. K. Richards

54-159

A Step Forward in Printing Telegraphy—A. S. Benjamin and W. J. Zenner. (*Communication and Electronics*, No. 11, pp. 10–15; March, 1954.) A new teletypewriter is described. Instead of type bars or wheels, the print mechanism in the new machine consists of a "type box" containing a 4- by 16 array of type heads. To print a character, the type box is appropriately positioned in front of the paper and a single hammer causes the type head to be driven against the paper. Typing speed is 100 words per minute. Various other technical features and operating advantages are pointed out and explained. Other units (tape printer, perforator, and reperforator transmitter) in a new line of equipment were mentioned.

R. K. Richards

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54-160

A New Digital Computer—(*Electronic Eng.*, vol. 25, p. 201; May, 1953.) A brief description is given of the Elliott Brothers (London) type 401 high speed general purpose digital computer, which was first exhibited in April, 1953. The machine was designed for commercial production, and uses the "sub-unit" principle of construction. A 1024-word magnetic disk memory is used in the first model, with plans to increase the size to about 3000 words in subsequent models. The original disk is 9 inches in diameter, rotates at 4500 rpm, and records 160 bits per inch; 8 tracks are used, each storing 128 words of 32 bits each. Machine size is $13' \times 2' \times 7\frac{1}{2}'$, including power supply, but not counting the operator's "trolley." A photoelectric reader is provided, for reading 5-hole teletype tape. The original model was built in only seven months.

R. G. Canning

54-161

LEO—Lyons Electronic Office—(*Electronic Eng.*, vol. 26, p. 162; April, 1954.) A brief announcement of an automatic digital calculator designed, built, and installed for their own use by J. Lyons and Co., London. Based on the EDSAC design, the machine has been modified for commercial clerical work by the use of higher speed input and output. Payroll, cost accounting and inventory control jobs are being done regularly, with other jobs in preparation. In addition, numerous scientific computations have been performed. Ferranti punched tape and Hollerith punched card inputs are provided, with output to a Hollerith printer and card punch. A 2048-word internal memory is mentioned indicating a binary mode of operation, and no mention is made of large volume tape memory.

R. G. Canning

54-162

The Circle Computer—John Greig. (*MTAC*, vol. VII, pp. 249–255 and frontispiece; October, 1953.) This article is a short description of a binary, stored program, magnetic drum computer. It is a single address machine, with a word length of 40 bits plus sign. The magnetic drum revolves at a speed of 3540 rpm. Hence the time necessary to execute an instruction and read the next order is 1.5 revolutions or 25 milliseconds. Multiplication and division take somewhat longer (45 msec). Input and output are by means of six-hole paper tape in parallel with a typewriter. Decimal to binary conversion and vice versa can be accomplished simultaneously with input and output. The electronic components are in small units attached with screw connections. Standard circuits and tubes are used, requiring no high currents. There were three computers in manufacture when the article was written. One has a 4096-word memory, which can be used as 8192 half words of six decimal digits each. The standard model has 1024 words of memory storage.

John Selfridge

621.375.2 54-163

The SWAC—Design Features and Operating Experience—H. D. Huskey, R. Thorensen, B. F. Ambrosio, and E. C. Yowell. (*Proc. I.R.E.*, vol. 41, pp. 1294–1299; October, 1953.) The SWAC was the first Williams tube computer to be completed in this country. Developed and built by the National Bureau of Standards, it is located at the Institute for Numerical Analysis, in Los Angeles. In addition to a 256-word electrostatic memory, the machine includes 4096 words of magnetic drum memory. At the time of writing, the SWAC's high speed, for handling the binary equivalent of 11 decimal digit precision (37 bits), was greater than any other computer in operation; for example, its add time is 64 μsec. During the summer of 1953, when the article was written, it was producing useful results during 70 per cent of power-on time, an enviable record even for later crt machines. Occupying some 62 square feet, the machine includes about 2600 tubes and 3700 crystal diodes, with a total power consumption of 30 KW. The article describes several unique features of the SWAC, including (a) the modified-four-address system used, where the address of the next instruction is obtained from the present instruction in case of an overflow on add, subtract, and multiply operations, and from the command counter otherwise; (b) an efficient method for transferring blocks of words between the crt and drum memories, with a per-word access time of 500 μsec; and (c) a high speed punched card collator input and card punch output. Operating on a two shift per day basis, the SWAC has completed a number of interesting problems, ranging from pure mathematics (a study of Mersenne numbers, related to the "perfect numbers" of the Greeks) to large volume data reduction problems (some 750,000 points of data reduced in 325 machine hours).

R. G. Canning

UTILIZATION OF DIGITAL EQUIPMENT

54-164

Subroutines: Prefabricated Blocks for Building—Margaret H. Harper. (*Computers and Automation*, vol. 3, pp. 14–15; March, 1954.) In order to be more efficient in producing programs, increased use will have to be made of large standard libraries of subroutines, which can be built up as a common effort of all programmers, perhaps utilizing the ability of computers to translate from one computer code to another to allow interchangeability between machines. Three kinds of subroutines exist: 1.) The static or passive subroutine, which needs only repositioning and conversion from relative to fixed addresses to be utilized in a computation. All other parameters are fixed. 2.) The dynamic or active subroutine, which contains instructions that cause modification of the subroutine during the process of compiling the main problem routine, according to the values of certain parameters. 3.) The generative subroutine which contains instructions that actually generate the subroutine which is finally to be placed in the main routine, according to the values of certain parameters supplied during the compiling of the main routine. Increasing use of these types of subroutines also requires the development of more comprehensive executive and compiler routines which will assemble a complete set of instructions for the problem solution, utilizing the various subroutines to help in this task.

G. E. Gourrich

681.142 54-165

Dead Programmes for a Magnetic Drum Automatic Computer—W. L. van der Poel. (*Appl. Sci. Res.*, vol. B3, pp. 190–198; 1953.) Breakdown due to a wrong instruction can be prevented by blocking part of the magnetic-drum memory for writing, and placing in this "dead" part standard subprograms which occur frequently.

Courtesy of *Proc. I.R.E.* and *Wireless Engineer*.

321.375.2 54-166

Diagnostic Programs for the Illiac—D. J. Wheeler, J. E. Robertson. (*Proc. I.R.E.*, vol. 41, pp. 1320–1325; October, 1953.) The Illiac is patterned after the Institute for Advanced Study Computer and is briefly described. Typical faults which can occur in a computer and their effects on computer operation are discussed. The uses of diagnostic programs for fault detection, fault isolation, and periodic computer servicing are discussed. Details of typical programs are presented. The need for diagnostic programs is stressed.

D. E. Hart

54-167

Digital Computers as an Aid in Electric-Machine Design—R. M. Saunders. (*Communication and Electronics*, No. 12, pp. 189–192; May, 1954.) This paper introduces digital computers to the designer of electrical machinery, particularly motors and generators. It is shown how digital computers make it possible to arrive at appropriate designs much more quickly than with manual methods and how it becomes possible in many cases to arrive at a better design. The major steps in the process are outlined, and sample calculations for an induction motor are given.

R. K. Richards

681.142:53 54-168

Application of Digital Computing Techniques to Physics—R. A. Brooker. (*Brit. Jour. Appl. Phys.*, vol. 4, pp. 321–326; November, 1953.) Problems involving matrixes, ordinary, and partial differential equations, functions occurring in crystallography and the "random walk" statistical method are discussed. Machine design and the training of personnel are considered briefly.

Courtesy *Proc. I.R.E.* and *Wireless Engineer*.

ORIENTATION READING

54-169

General Purpose Robots—Lawrence M. Clark. (*Computers and Automation*, vol. 3, pp. 22–25; April, 1954.) There are many situations existing in our civilization that provide suitable applications for a general-purpose robot, which would resemble a human being in many ways but would be even more versatile or general-purpose. A robot is a machine with a perceptive apparatus, an acting apparatus, and a programming apparatus, assembled together in an operating entity so that it may take some kind of appropriate action depending on its percep-

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tion of its environment. Many special-purpose robots are in common use, such as the "responsive" traffic light, but general-purpose robots will be much more practical when they are to be used in a number of different applications from time to time. The author predicts many properties of these general purpose robots, explaining how a few of them could be attained. It is concluded that much engineering work and miniaturization of hardware must take place before such robots can exist. However, as robots are gradually developed having n abilities, these can be combined in 2^n ways, having more versatile application than human beings having all abilities in one package.

G. E. Gourrich

54-170

Processing Information Using a Common Machine Language: The American Management Association Conference, February 1954—Neil Macdonald. (*Computers and Automation*, vol. 3, pp. 6–7, April, 1954.) A special conference of the American Management Association, held in New York, February 25 and 26, subject, "Integrating the Office for Electronics," included a presentation of the philosophy and equipment mechanization of the United States Steel Corporation's "Integrated Data Processing" procedures. These procedures make use of several "common language" machines which perform the required data processing functions without the necessity of copying the information to perform translation from one machine language to another after the initial transcription at the point of origin. Data is initially recorded on a five-channel punched tape and subsequent processing is completely automatic. This note lists the papers concerned with this topic and the exhibited machines which carry out the processing. The talks are to be printed in *Office Management*.

G. E. Gourrich

54-171

The Influence of Automatic Computing Machines on Mathematical Research—H. D. Huskey. (*Industrial Mathematics*, vol. 4, pp. 39–48; 1954.) This is essentially an expository article dealing with the design and use of high-speed computers, and with their influence on pure and applied mathematics. The author discusses some of the latest computer design features and their uses as well as possible future trends in this field. The article concludes with some applications of computers to problems in pure and applied mathematics.

S. D. Conte

54-172

Autonomy and Self-Repair for Computers: A Symposium—Elliot L. Gruenberg. (*Computers and Automation*, vol. 3, pp. 12–13; May, 1954.) The author presents a summary of the symposium held in New York, March 25, 1954, at the meeting of the PGEC, on the subjects: 1) Can computers be made more autonomous? 2) Can computers be made to repair themselves? Such topics were discussed as: Making machines of more reliable components; designing computers which do not break down when individual components fail; using one computer to repair another; building machines to interpret written formulas and perform mathematical analysis directly; use of a computer to organize its own data, such as in automatic programming; the differences between computers and the nervous system of the higher animals; designing machines which understand human language. Several speakers pointed out what should be done to make present machines more useful before worrying about autonomy. Some general comments on the meeting are included. The paper concludes, "none of the scientists present took the view that machines should autonomously do problem solving or problem finding . . . the speakers . . . thought more in terms of a slave machine that ought only to take orders, give no trouble, and keep itself in good repair." (Editor's note—In this article W. B. Huskey should read H. D. Huskey.)

G. E. Gourrich

BOOK REVIEWS

54-173

Le Calcul Analogique (Principles et Contribution à une Théorie Générale)—F. H. Raymond. (*Societe d'Electronique et d'Automatisme*, 134 pp.; 1953. In French.) This book is a collection of lectures given by M. Raymond in May, 1952 at L'Institut National Pour Les Applications Du Calcul at Rome. The book admittedly draws heavily on the computer literature of the United States for its contents but calls to our attention the work the French are doing in this field. *Introduction*. The fifteen page introduction gives a brief survey of the development of the field of mathematical machines. The influence of these machines on human relations is of some concern to M. Raymond. He relates the principle of "feedback" to the more general concept of "cybernetics" of N. Wiener fame. (He mentions however that Ampere invented the word.) A social analog of feedback is given as, "A modern democracy is a feedback system where the legal means of altering the government represents the feedback loop. There is no feedback in a dictatorship." The introduction continues with mention of Lord Kelvin; V. Bush and his mechanical computer; digital computers and how they differ from analog computers. *Chapter I: Principles of Analog Computing*. The Laplace transformation techniques are introduced for solving sets of linear differential equations and loop equations. Electric and electronic methods of addition, multiplication, division, integration, differentiation, and function generation are reviewed. The chapter describes the Bell Telephone Company computer, Leeds Northrup, Philbrick, the "Anacom" of Westinghouse, "Typhoon" of RCA, "Gepus" of the Royal Aircraft and the "OME-12," the French machine of the Societe D'Electronique Et D'Automatisme. *Chapter II: Operation of Analog Computers*. This chapter discusses linear algebraic equation solvers using matrix theory and notation to present the methods of solution. The Consolidated Engineering Company machine and the OME-11 of S.E.A. are described. Systems of linear differential equations are solved with electronic analog computers using matrix notation with the circuit symbols familiar in United States literature. Finally a second order differential equation is solved by reducing it to a system of first order equations. *Chapter III: Electronic Mathematical Operators*. Chapter III discusses the elementary mathematical operators concerned with passive networks, shows their physical analogs as transfer functions, and extends this technique to the solution of systems of linear differential equations and to an nth order differential equation. *Chapter IV: Accuracy and Stability*. Chapter IV discusses precision and stability of analog computers; presenting formulae for establishing the precision of a certain solution on the French OME-111. Stability criteria are developed, with the help of Nyquist diagrams, for linear algebraic equation solvers and for differential analyzers.

Cyril P. Atkinson

54-174

Automatic Digital Calculators—A. D. Booth and K. H. V. Booth. (*Butterworths Scientific Publications*, London, 230 pp.; 1953.) In their preface, Dr. and Mrs. Booth state that they intend their book to be a guide to the theory of automatic calculators, introducing new workers in the field to the notions, language, and literature of the subject. They begin with a short history of mechanical and electronic computers, and continue with chapters on the principal parts of these machines—the control, the arithmetic unit, the memory, and input-output devices. Sections on electronic, magnetic, and relay circuits follow. Several chapters on coding and programs are included next, and the book ends with a discussion of some applications of the machines. However, though the book contains a great deal of information and an excellent bibliography, it invites criticism principally on the grounds that it omits so many important points and differs in so many respects from widely accepted current practice. Omissions are easy to point out. The chapters on circuit design hardly mention the cathode follower, and leave out any discussion of the importance of circuit stability to reliability. The use of mathematical techniques in logical design is ignored. The concept of interpretive subroutines is not explained, though the authors discuss floating-point routines (see below). One other omission is particularly disappointing: that ingenious British invention, the "B-box," is nowhere mentioned. Since a beginning book cannot be expected to explain everything, some of the omissions may be justified. However, the authors also present many statements or arguments which are incorrect, incomplete, or misleading. It is not correct that " . . . negative numbers are invariably stored in complement form" (p. 44). It is at least questionable whether " . . . from the point of view of simplicity (in coding) the one-address code is undoubtedly preferable . . . " (p. 137). The statement, made on p. 169, that floating-point routines should be regarded as a last resort "rather than as an easy alternative to careful planning," will provoke considerable controversy. The chapters on programing emphasize the techniques of interpolation for use in evaluating basic functions, without adequately comparing these techniques with others more widely used. In short, the book would not seem to be a very reliable guide for newcomers to the field, though it will be of interest to the initiated.

Montgomery Phister, Jr.

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—*The Editor*

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